REPORT No. CR-63-547-31

THIRD QUARTERLY INTERIM TECHNICAL REPORT

15 FEBRUARY 1963

MULTISYSTEM TEST EQUIPMENT

CONTRACT DA-36-034-ORD-3650 RD

UNITED STATES ARMY MISSILE COMMAND

AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION

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Contract DA-36-034-ORD-3650 Z
MULTISYSTEM TEST EQUIPMENT

Prepared for:

COMMANDING GENERAL
ARMY MISSILE COMMAND
REDSTONE ARSENAL, ALABAMA
ATTN: AMSHI-RHD

Prepared by:

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DEFENSE ELECTRONIC PRODUCTS
AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION
BURLINGTON, MASSACHUSETTS

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FOREWORD

Radio Corporation of America submits the Multisystem Test Equipment Third Quarterly Interim Technical Report, in response to the requirements of paragraph 7.3 of TR 160 Revision No. 3, dated 29 January 1962.

This report is submitted to Army Missile Command Redstone Arsenal, Alabama under Contract DA-36-034-ORD-3650 Z, ATTN: AMSMI-RHD.

This quarterly report covers the period from 1 October 1962 to 31 December 1962.

REPORT APPROVAL

This Third Quarterly Interim Technical Report has been reviewed and approved by:

R. B. Barnhill, Manager
MTE Programs

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

SECTION 1

INTRODUCTION

During the past quarter, work was concentrated on the Multisystem Test Equipment (MTE) design and development effort.

The system design effort placed emphasis on the completion of group and assembly specifications and finalizing shelter layouts. In the equipment design and development area, design of subsystems for the Electronic Test Set was completed and detailed development initiated. The subcontractor for the Hydraulic Test Set (HTS) was approved and a detailed investigation of servovalve testing conducted. Also, a study of hydraulic fluid contamination effects both within the HTS and Mauler was completed.

TDO-MTE-1 through 8 were received, evaluated, and required actions completed. The computer recommended in the Computer/Controller Study Report (CR-62-547-12) was approved by the Army Missile Command; a description of the Computer/Controller is included in this report. The MTE Characteristics Study Report No. 2 and a revised set of Preliminary Purchase Description were completed and submitted to the Army Missile Command.

SECTION 2

STUDIES AND PRESENTATIONS

2.1 TEST REQUIREMENTS ANALYSIS (TRA)

2.1.1 TRA REPORT

Test Requirements Analysis Report, CR-62-547-27 was issued 6 December 1962. The report covers analysis of missile system data received by RCA prior to 1 November 1962.

To the extent of available information, the report contains generation breakdowns at major assembly level, tabulated data parameters at subsystem level, and data correlation charts. Common and peculiar test requirements are determined from the correlation charts.

A tabulation of units-under-test (UUT's) indicates that 86 percent of UUT's analyzed are adaptable to automatic testing. A test-time flow chart for a typical UUT is included in the TRA Report.

The Mauler Missile System has received top TRA priority. Although less than half of the Mauler UUT's are adequately described by available documentation, a spectrum of Mauler test requirements has been developed by extrapolation and engineering estimates. The test requirement data will be verified and expanded as additional Mauler documentation is received.

2.1.2 TRA DOCUMENTATION

Missile sytem documentation received during the report period is listed in Table 2-1.

Table 2-1. TRA documentation received during quarter

Missile System	Reports	TM's	Schematics	Test Procedure	RMOC's	Specs.
Mauler	17		342	4		6
Nike Zeus			33	31	11	
Sergeant		34	137	7		10
Pershing	8		112			
Hawk		8	42			
Nike Hercules		21	334	15		
La Crosse		3	3			

RCA requested missile-system documentation from Army Missile Command during the report period as follows:

RCA Letter No.	Date	Missile System
ECR:MTE:117	20 Oct.	Pershing Mauler Nike-Hercules
ECR:MTE:124	13 Nov.	Hawk
ECR:MTE:142	17 Dec.	Hawk

2.1.3 TRA PLANS

TRA effort will continue as data is received. The status of TRA documentation will be evaluated in detail. Specific requests will be initiated for data necessary: (1) to adequately support test programming effort, and (2) to identify Mauler design changes between the engineering and prototype models.

2.2 CONTACT SUPPORT UNIT (CSU) STUDY

A proposed CSU configuration and deployment philosophy was covered in MTE Characteristics Study Report, CR-62-547-15 (6 September 1962). In accordance with Army Missile Command redirection, a revised CSU configuration is proposed consisting of an Organic CSU and a Missile CSU.

The Organic CSU includes test equipment selected from the Electronic Test Unit complement. Mission requirements have been extrapolated from limited data available on Mauler 1st and 2nd echelon maintenance capability. Test flow charts have been prepared to indicate fault-isolation sequence down to replaceable sub-assemblies. Detailed information of Mauler self-test and 2nd echelon test and repair capabilities was not available.

The Missile CSU includes test equipment necessary to perform pre-issue checkout of missiles at ammunition supply points (ASP and SASP). Present configuation includes capability to fault-isolate Mauler and Shillelagh missiles down to replaceable sections or assemblies. Test flow charts have been prepared for testing missiles either in or out of canisters.

A CSU Study Report will be issued during the next reporting period. After RCA obtains guidance from Army Missile Command and data on Mauler test and repair capability CSU technical and operational requirements will be established to satisfy MTE Qualitative Materiel Requirements (QMR).

2.3 REPAIR SUPPORT UNIT (RSU) STUDY

This study will establish requirements for supplemental repair facilities within the direct and general support field maintenance shop

implemented with MTE. A preliminary RSU Study Report will be issued during the next report period.

A study team of RCA and Army Missile Command personnel visited missile support sites in the United States during December 1962. They inspected existing repair facilities and documented interviews with maintenance personnel.

Questionnaires have been sent to all overseas Army Missile Support organizations by Army Missile Command Supply and Maintenance Directorate. Replies to these questionnaires will supplement data obtained by personal interviews conducted with maintenance personnel within the United States.

RSU Study effort will be extended to complete analysis of configuration requirements and recommanded complement of tools.

2.4 TEST PLAN FORMULATION

The objective of the MTE Test Plan is to establish a composite plan for all tests to be performed on deliverable equipment through final field acceptance tests. Tests will be performed at all levels of assembly starting at the printed circuit board level.

The detailed Test Plan presently being prepared applies to the MTE Developmental Model. A generalized MTE Test Plan, formulated during this report period, is shown as a flow diagram in Figure 2-1. Test phases covered in the flow diagram are briefly described here.

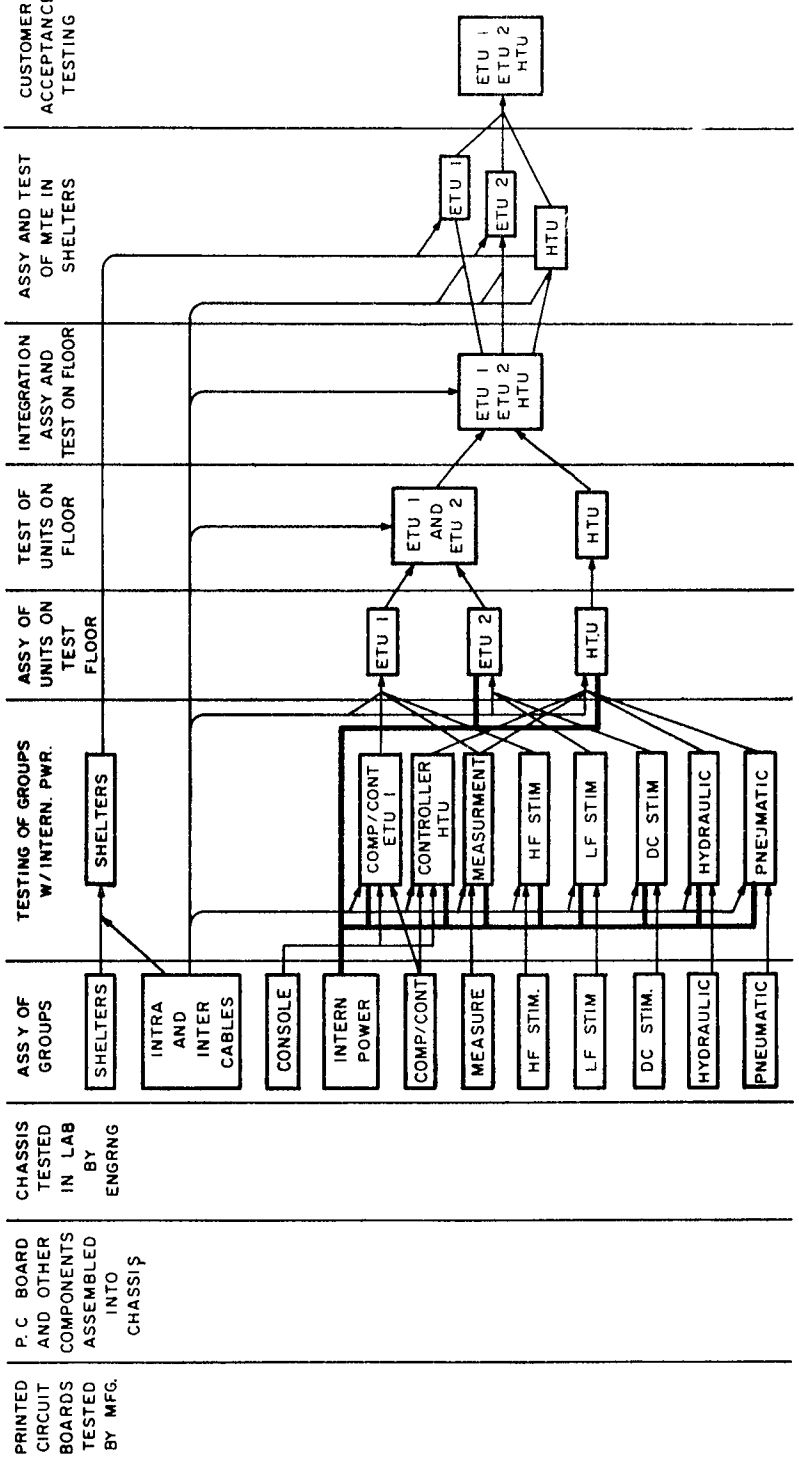


Figure 2-1. Generalized MTE test plan

Printed circuit boards will be tested by the manufacturing facility and will be forwarded to chassis assembly with a high level of confidence already established.

Once the individual chassis have been assembled, the cognizant engineering design group will perform laboratory testing.

Upon satisfactory completion of the laboratory test program the chassis will be assembled into racks and tested as functional groups, i.e., Computer/Controller, HF Stimulus, using MTE internal power. During this phase of testing, self-test tapes will be used as feasible.

As each functional group completes the isolated test phase, it will be combined with other functional groups for integration into Units. Units will be built up in a logical functional sequence (Computer/Controller group, Measurement group). Units will be assembled on the test floor in their normal physical configuration, but will not be installed in the shelters at this point.

As each unit is completed and thoroughly tested, integration testing of the overall MTE system will commence. Self-test tapes will be used; control of the entire system will be maintained from the Computer/Controller in Electronic-Test Unit 1 with the Hydraulic-Test Unit in the Remote-Automatic mode of operation. This phase of the test program will confirm the integrated operation of MTE including satisfactory operation with respect to EMI and RFI. At the completion of the integration test phase the racks will be assembled in the shelters and the integration test program will be repeated. The MTE System will then be ready for Customer Acceptance Testing.

During the next report period the Test Plan will be expanded in sufficient detail to definitize a time scale and to establish an explicit test and integration operational sequence.

2.5 DESIGN CHARACTERISTICS REVIEW

A Design Characteristics Review is scheduled by the Army Missile Command to take place on the 15th and 16th of January 1963. The purpose of this Review is to assure that all aspects of the MTE Program are completely coordinated. RCA is responsible for preparation and review of the DCR material coordinated by Missile Command Directorates, and for providing technical support for the Review.

Presentation material for the Design Characteristics Review was generated and coordinated by the Army Missile Command. The Design Characteristics Review was published in December 1962 and copies distributed as directed by the Army Missile Command. Presentation slides were prepared and delivered to the Army Missile Command. A set of display mockups was prepared to be used in support of the Design Characteristics Review. Mockups consist of:

Electronic Test Unit 1	(Full scale in heli-hut)
Electronic Test Unit 1	(1/4 scale)
Electronic Test Unit 2	(1/4 scale)
Hydraulic Test Unit	(1/4 scale)
Pneumatic Test Unit	(1/4 scale)

Sand Table Display with scale models of MTE Direct Support Shop Set and Contact Support Units.

During the next quarter, the MTE mockups will be delivered to the Missile Command, Huntsville, Alabama for display during the Design Characteristics Review. RCA engineering personnel will support technical discussions. The Design Characteristics Review brochure will be updated according to policy changes determined during the DCR.

2.6 MTE CHARACTERISTICS STUDY REPORT NO. 2

A supplement to the MTE Characteristics Study Report, CR-62-547-15, submitted 6 Sept. 1962, was prepared. This Report, "Multisystem Test Equipment System Study Report No. 2," (CR-62-547-29) contains a detailed description of the MTE system and equipment.

A revised set of Preliminary Purchase Descriptions (specifications) covering the MTE System, was submitted on 31 December 1962.

SECTION 3

DESIGN

3.1 SYSTEM DESIGN

3.1.1 OBJECTIVE

(1) To verify the group and assembly specifications and descriptions to allow completion of equipment design and to allow final assembly design.

(2) To establish shelter layouts to allow the shelter design to progress.

3.1.2 PROGRESS

A. Shelter Layouts

The arrangement of the equipment groups in the Electronic Test Unit shelters was re-examined. The basic configuration shown in the last quarterly report appears to be the best compromise. Some of the higher frequency signals of the Low Frequency Stimulus Group must be sent from ETU-2 to ETU-1. This requires special line drivers, which can be kept to a minimum.

There has been no alteration of the equipment configuration in the Hydraulic Test Unit during the period.

B. DC Stimulus Group

The maximum current capability of the 0-36 volt programmable power supplies has been raised from 10 to 15 amperes to satisfy TRA requirements.

C. Internal Power Supply Group

No changes required.

D. Measurement Group

Refinements in the Measurement Group resulted in basic improvements in the following areas.

a. Analog Measurements

The method of successive approximations has been chosen for analog measurements. The analog-to-digital converter (ADCON) has a single ended input, and all isolation is accomplished in the appropriate converters. This facilitates the design of the ADCON.

The RF probe for voltage measurements over the frequency range of 10 kc to 100 Mc has been redefined to allow high impedance measurements in addition to 50 ohm input. This increases the versatility of the system.

b. Frequency Measurements

A high impedance input has been added to both input channels of the Time Interval and Frequency Converter for use in frequency measurements as well as time interval measurements for signals in the range of 20 cps to 10 Mc. Previously, only a 50 ohm input impedance was available on both the 20 cps to 10 Mc range and 10 Mc to 100 Mc range. This change permits frequency/time measurements on high impedance sources without special signal conditioning in the testing of digital and pulse circuits.

c. Test Point Selection

A feature has been added to the Monitor Adapter whereby low frequency testpoints may be monitored by the RF probe as well as by coaxial test points. Previously the probe could monitor only the ten coaxial test points allotted to the B matrix. This change was made in conjunction with the RF probe change, mentioned in paragraph (1) above. Flexibility of the probe is increased by providing more test points and permitting high impedance RF voltage measurements at relatively low frequencies.

The maximum allowable current for low frequency test points was lowered from 500 Ma to 300 Ma to permit the use of a special low-capacitance shielded wire within the Monitor Adapter. This change will improve the performance of the Measurements Group without limiting measurement capability; 300 Ma is well above the worst case test point current drawn by this equipment group.

E. High Frequency Stimulus Group

The systems activity in the High Frequency Stimulus Group consisted of repackaging. Functions were grouped into more appropriate assemblies to facilitate interconnection and to allow greater use of building blocks.

Figure 3-1 shows the new rack layout for the High Frequency Stimulus Group. Comparison with the previous rack layout points out the following differences:

(1) The X-Band Input and the X-Band Output have been combined into a single chassis to reduce interconnections.

(2) The L-Band Ratiometer has been combined with the L-Band Conversion into a single chassis to reduce interconnections.

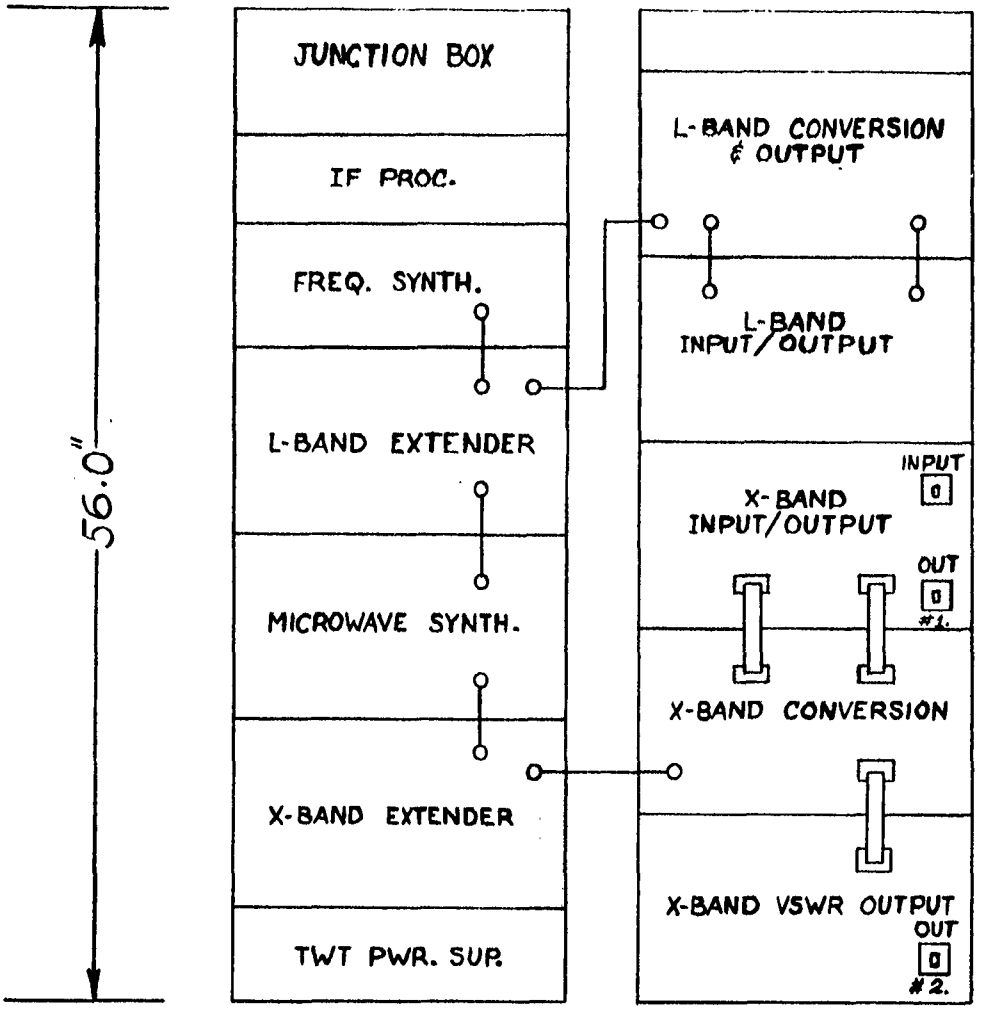


Figure 3-1. High frequency stimulus group - rack configuration

(3) The Microwave Synthesizer, which was formerly part of the X-Band Frequency Extender, is a new assembly. This change reduces interconnections.

(4) The Bandpass Filter power supply chassis is no longer required; the rejection of the single side band modulators obviates the need for electronically-controlled bandpass filters.

F. Low Frequency Stimulus Group

(1) The lower frequency limit of the AF/RF Generator was changed to 100 cps from 1 kc as a result of the TRA.

(2) The programmable increments of the RF synthesizer were increased from 10 cps to 100 cps as a result of TRA information. Increasing the increments in this manner facilitates synthesizer design.

(3) The stability of the frequency standard was reduced from 0.5 parts in 10^{11} rms/sec to 1 part in 10^{9}/sec. The system under test does not require the 5 part in 10^{11} stability previously reported. This change facilitates procurement and testing of the assembly.

G. Computer/Controller Group

During the past quarter, RCA received and complied with TDO-MTE-3 and TDO-MTE-5. TDO-MTE-3 requested additional technical data and costs on the tape punch; drawings, instruction books, and costs were submitted. TDO-MTE-5 requested additional data on the tape reader, printer, visual instructor, and displays. The requested data was submitted with a list of recommended displays meeting the MTE requirements.

The C/C group has not been described in detail in previous Quarterly Technical Reports. Since the Computer recommendation was approved by the Missile Command during this quarter, a complete description of the Computer Controller is presented in Appendix A.

SECTION 4

STANDARDS DESIGN AND DEVELOPMENT

4.1 STANDARD CIRCUITS

4.1.1 GENERAL

Standard circuits effort can be divided into two parts:

(1) design and development of standard millimodule circuits such as Gates, and Flip-Flops; and

(2) design and development of standard functional cards which contain combinations of the standard millimodules.

The effort included an initial survey of presently known standard circuit and functional card requirements for the MTE equipment.

The reporting period was largely spent in design and development of standard millimodule types. A maximum allowable power dissipation of 400 mw per module, the same as allowed for standard RCA micromodules, has been chosen so that the millimodules can be converted to micromodules at some future date with a minimum of effort.

Allocation of functions to printed circuit card standards was started and should be completed during the next reporting period.

4.1.2 BASIC REQUIREMENTS CONSIDERED IN CHOSING STANDARD MILLIMODULE CIRCUITS

The following basic requirements affecting all of the circuits were considered:

(1) Temperature range
(2) Type of semiconductor device-silicon vs germanium
(3) Type of transistor - PNP vs NPN
(4) Type of logic
(5) Logic levels
(6) Logic functions required
(7) Speed of operation
(8) Power supply voltages
(9) Noise immunity

The conclusions concerning these requirements and contained in the following paragraphs apply to millimodule circuits used generally throughout MTE. Specialized requirements may require some deviation from the basic ground rules established.

A. Temperature Range

MTE overall specifications call out the following temperature requirements:

Storage: $-53.9^{\circ}C$ to $+71.1^{\circ}C$
Operating: $-18^{\circ}C$ to $+51.7^{\circ}C$

The millimodules will not be subjected to operating temperatures below those specified. However, they will be subjected to operating temperatures higher than those contained in the overall specification because of temperature rise of the cooling air. The temperature specifications placed upon the millimodules were, therefore,

Storage: $-53.9^{\circ}C$ to $+71.1^{\circ}C$
Operating: $-18^{\circ}C$ to $+68^{\circ}C$

B. Types of Semiconductor Devices

Silicon and germanium semiconductor devices were compared. The upper operating temperature limit of +68°C is sufficiently close to the upper temperature limits of most germanium transistors to significantly degrade reliability.

An additional temperature rise of at least 10°C can be expected within the potted millimodules. These considerations, plus the fact that AM 3100 logic circuits using silicon transistors have already been designed and tested, led to a decision strongly favoring silicon semiconductors.

C. Type of Transistor - PNP vs NPN

NPN silicon transistors are easier to manufacture, more readily available, and less expensive than PNP silicon transistors. In addition, 10 Mc switching speeds are required in some parts of MTE, and no reliable PNP silicon transistor capable of operation at that speed was available. It was therefore decided to use NPN transistors except where circuit considerations made the NPN unsuitable.

D. Type of Logic

A number of types and variations of logic circuits could have been selected as standard for MTE. Some types considered were:

direct-coupled transistor logic,
resistor-transistor logic
multiple-level diode logic
resistance-coupled complementary transistor logic
diode-transistor logic

Considered in the selection were relative cost, power dissipation, noise immunity, circuit simplicity, switching speed and load capacity.

No one type is best in each area for all applications, but, because of good all around performance, diode transistor logic (DTL) was selected to be added to the MTE standard circuit inventory. DTL permits simple and reliable circuitry where registers and counters constitute the bulk of digital circuits, as in the controller and other MTE subsystems.

E. Logic Levels

The selection of voltage levels to represent binary quantities requires optimization of a number of variables. The most important of these are: cost, switching speed, power dissipation, and vulnerability to noise. Lowering the voltage level favors all other requirements at the expense of increasing noise vulnerability; conversely, raining voltage level has the opposite effect. High switching speeds and logical voltage levels over 6 volts are a particularly bad combination because of the scarcity and cost of transistors for that application.

All things considered, 0 and +6 volts, representing logical "0" and "1" respectively, were finally selected for MTE switching circuiting. This level will provide the proper degree of noise immunity for switching control signals, which must often be sent over long cables.

F. DC Power Supply Voltages

It was decided to standardize on dc power supply voltages preferred by both the Military and by RCA - DEP Central Engineering (Standards). The following voltages taken from MIL-STD-706A were made available for selection by circuit designers.

+1.5; ±3; ±6; ±12; ±25; ±50; ±100; ±150; ±250; ±300; ±450; and ±600 vdc.

For logic and control circuitry, this list has been reduced to:

±3, ±6, ±12, ±25 and ±50 vdc.

Circuit design requirements were also established to allow a ±5 percent tolerance on these supply voltages.

G. Noise Immunity

To minimize the effect of capacitive pickup on logic signal lines, clamp diodes will be used at the output of logic circuits as required and where consistent with power drain and switching speed.

H. Speed of Operation

Logic circuit operation at speeds up to 10 Mc will be required. Because of the different designs (and higher prices) of transistors required in logic circuits operating at speeds above 1 Mc, the standard logic circuits were divided into two groups: medium speed - dc to 1 Mc; and high speed - dc to 10 Mc (generally used only at speeds from 1 Mc to 10 Mc).

4.1.3 CIRCUITS UNDER DESIGN

The major part of the design effort to date has been expended on the circuits that will be used most often in the MTE Equipment. These circuits are:

(1) Medium Speed NAND/NOR Gate (MM101)
(2) Medium Speed Control Flip-Flop (MM103)
(3) Medium Speed Complementary Flip-Flop (MM104)
(4) Medium Speed Diode Cluster (MM107)
(5) High Speed NAND/NOR Gate (MM108)
(6) High Speed Control Flip-Flop (MM109)

(7) High Speed Complementary Flip-Flop (MM110)

(8) High Speed Diode Cluster (MM111)

(9) Relay Driver (MM106)

The goal has been to minimize the number of millimodule types. Accordingly identical millimodules are used for the medium speed NAND/NOR Gate and medium control Flip-Flop, the high speed NAND/NOR Gate and high speed control Flip-Flop, and the medium and high speed diode cluster. In addition, electrical parts are standardized for different millimodules to the extent practicable.

4.1.4 CIRCUIT DESIGNS

The status of the standard circuit designs is as follows:

A. MM101/MM108, Medium Speed NAND/NOR Gate and High Speed NAND/NOR Gate Millimodules

These millimodules when used as a NAND/NOR Gate consist of two independent NAND/NOR Gates. Each Gate has two diode inputs plus an additional cluster input to which additional diodes can be connected to expand the fan-in capabilities of the gate. The standard gates are called NAND/NOR because a NAND gate can be used as a NOR gate merely by interchanging the logical voltage levels. However, no such logic level interchange will occur within MTE; therefore these will provide NAND functions only.

The schematic diagram for the two NAND/NOR Gates contained in the millimodule is shown in Figure 4-1. The tentative characteristics for each gate are shown in Table 4-1. When either one or all of the inputs are at 0 v the transistor is cut off and the output is +6 v. When all of the inputs are at +6 v the transistor conducts and the output is at 0 v.

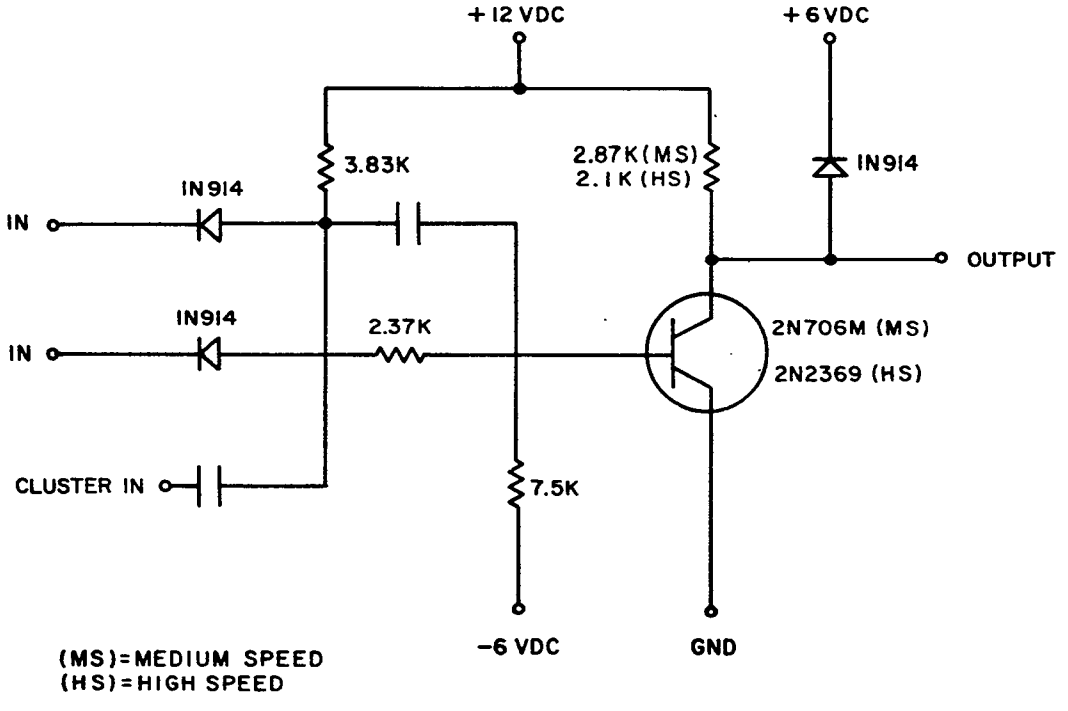


Figure 4-1. NAND/NOR gate millimodule (high speed and medium speed)

Table 4-1. Tentative characteristics (each gate)

Signal Inputs	High Speed	Medium Speed
Amplitude	0 to +1v	0 to +1v
	+6 ±1v	+6 ±1v
Rise Time	≤ 0.025 μsec	≤ 0.25 μsec
Fall Time	≤ 0.025 μsec	≤ 0.25 μsec
Pulse Width	≥ 0.05 μsec	≥ 0.5 μsec
Frequency	dc to 10 Mc (max)	dc to 1 Mc (max)
Input Impedance	1 gate load*	1 gate load*
Fan in	-------20------- (with external diolde cluster)	

Signal Output	High Speed	Medium Speed
Amplitude	0 to +1v	0 to +1v
	+6 ±1v	+6 ±1v
Rise Time	≤ 0.20 μsec	≤ 0.1 μsec
Fall Time	≤ 0.20 μsec	≤ 0.1 μsec
Storage Time	≤ 0.01 μsec	≤ 0.03 μsec
Delay Time	≤ 0.01 μsec	≤ 0.04 μsec
Load	3 gate loads (max)	4 gate loads** (max)

* One Gate load is defined as shown in Figure 4-2.

** Four Gate loads are defined as shown in Figure 4-3.

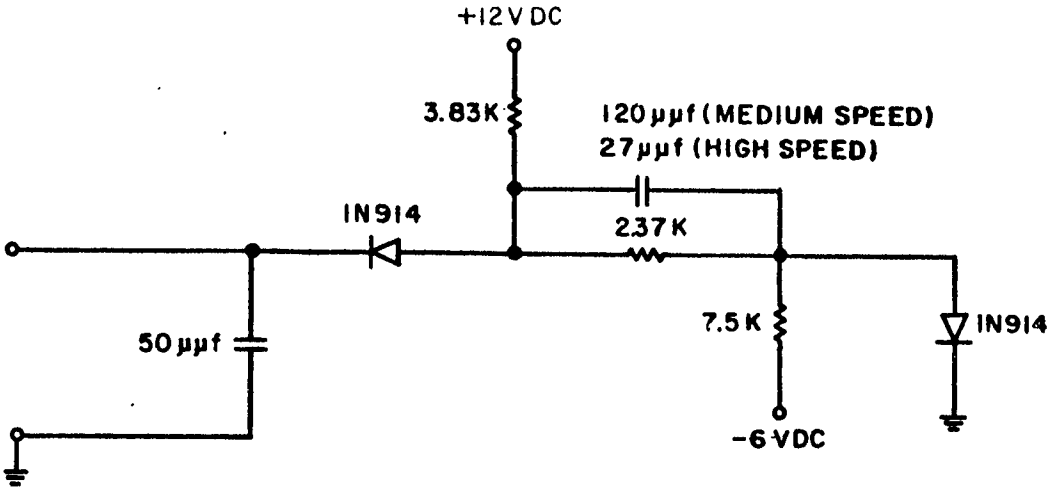


Figure 4-2. One gate load

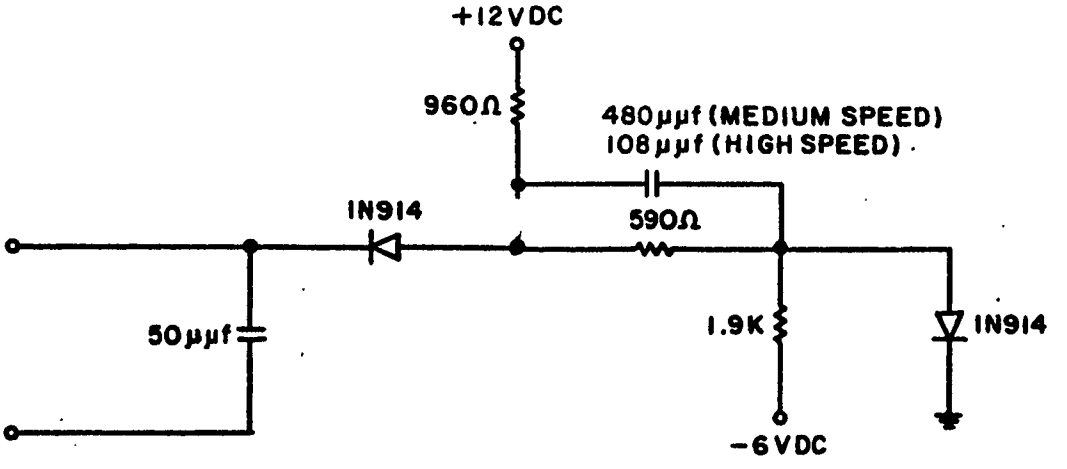


Figure 4-3. Four gate load

B. MM103/MM109 Medium Speed and High Speed Control Flip-Flop Millimodules

The Schematic Diagram for the Control Flip-Flop Millimodules is shown in Figure 4-4. This control Flip-Flop function is formed by use of the NAND/NOR gate millimodule with the output of each of the gates externally connected to an input of the other. Both the Set and Reset inputs of the control Flip-Flop are normally held at +6 volts. The Flip-Flop is set by applying a negative going 6 volt pulse (0 v level) to either the Set or Reset input while the other input is held at +6 v.

C. MM104/MM110 Medium Speed and High Speed Complementary Flip-Flop Millimodules

The Complementary Flip-Flop Millimodule Schematic Diagram is shown in Figure 4-5. This millimodule employs the same circuitry as does the Control Flip-Flop and in addition incorporates CRD (capacitor-resistor-diode) gates to allow operation as a shift register or counter. In the interest of a higher packaging density, present efforts are directed toward packaging this complete circuit in one millimodule. Due to space limitation, however, there is some possibility that the CRD gate portion may have to be packaged separately.

Parts common in function to the NAND/NOR gates and control flip-flops have the same values as their counterparts in the circuits previously discussed.

The trigger input of the flip-flop is a negative 6 volt pulse. When both the level set and level reset inputs are held at +6 volts, the trigger has no effect. When one of the level inputs is placed at 0 volts, the trigger is coupled to the corresponding transistor base to set the flip-flop in the desired state. The set and reset inputs operate as in the control flip-flop.

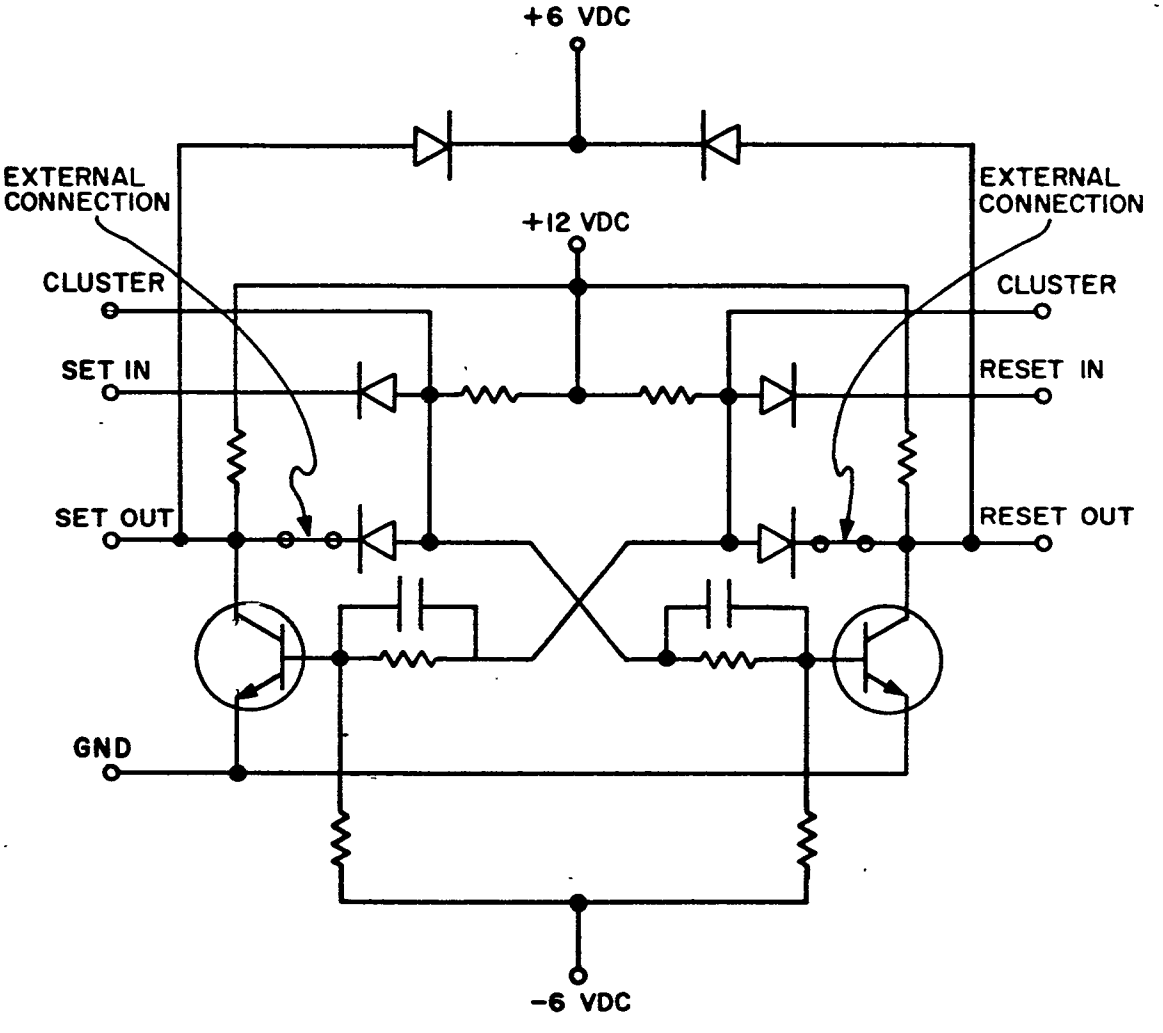


Figure 4-4. Control flip-flop - NAND/NOR gate millimodule with external connectors as indicated

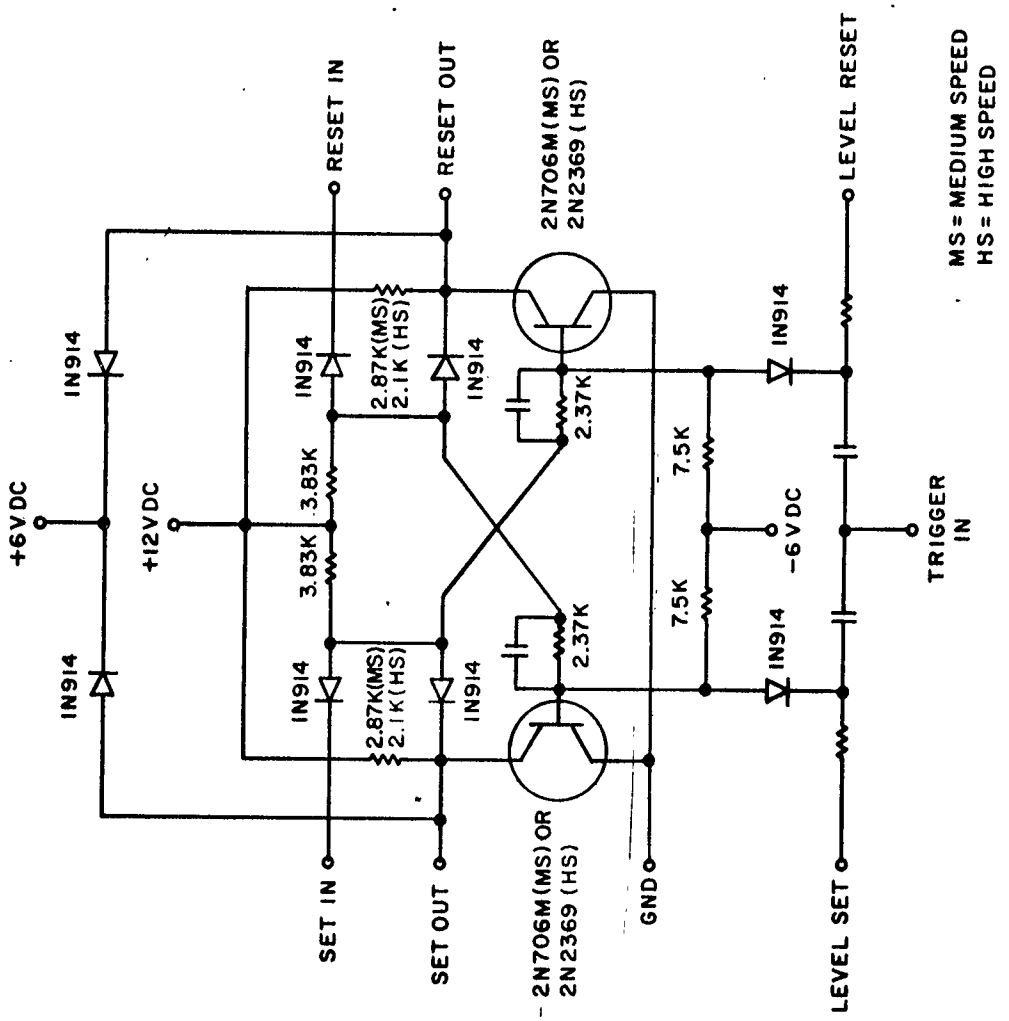


Figure 4-5. Complementary flip-flop

When the millimodule is used as a shift register the level set and level reset inputs come from an external circuit.

When the unit is used as a counter the level set and level reset terminals are connected to the Set out and Reset out terminals respectively. Each trigger pulse then causes the flip-flop to change state. Tentative characteristics for the flip-flop are shown in Table 4-2.

Table 4-2. Tentative characteristics - complementary flip-flop

	High Speed	Medium Speed
Trigger Input:		
Waveform	--- Negative pulse ---	
Amplitude	6 ± 1 v	6 ±1 v
Rise Time	≤ 0.020 μsec	≤ 0.2 μsec
Fall Time	≤ 0.020 μsec	≤ 0.2 μsec
Pulse Width	≥ 0.030 μsec	≥ 0.1 μsec
Frequency	≤ 10 Mc	≤ 1 Mc
Level Set and Reset Inputs:		
Waveform	essentially a constant level during the trigger input time.	
Amplitude	0 to + 1 v	0 to +1 v
	+6 ±1 v	+6 ±1 v
Set and Reset Inputs:	Same as for control flip-flop and NAND/NOR Gate signal inputs	
Signal Outputs:		
Amplitude	0 to +1 v +6 ±1 v	0 to +1 v +6 ± 1 v
Rise Time	≤ 0.020 μsec	≤ 0.1 μsec
Fall Time	≤ 0.02 μsec	≤ 0.1 μsec
Storage Time	≤ 0.01 μsec	≤ 0.03 μsec
Delay Time	≤ 0.01 μsec	≤ 0.04 μsec
Load	≤ 2 gate loads	≤ 3 gate loads

D. MM107/MM111 Medium Speed and High Speed Diode Cluster Millimodule

The diode cluster millimodule schematic diagram is shown in Figure 4-6. This millimodule is used in conjunction with the medium and high speed NAND/NOR gates (cluster input) to expand the fan-in of these circuits when necessary.

E. MM106 Relay Driver Millimodule

The relay driver millimodule design is being evaluated. Tentative selection of a circuit has been made; see Figure 4-7.

Breadboard models of all the millimodule circuits discussed have been constructed and have exhibited satisfactory operation in the laboratory.

Numerous variations of the basic configurations shown are possible. For example, the NAND/NOR gate millimodule could be constructed with 3 diode and one cluster input in one of the gates and two diodes inputs in the other, or the diodes in the diode cluster millimodule could be grouped singly, by 3's, 4's or a combination thereof, depending upon circuit requirements. Such configurations can be easily constructed without any further design effort other than minor packaging changes.

However, in the interest of having an absolute minimum of different types of millimodules used in the MTE, an established ground rule is that all MTE design groups must use only the configurations presented above. Deviation from this ground rule will occur only if future applications of those millimodules indicate that variation from the basic configurations will result in significant savings in space or cost.

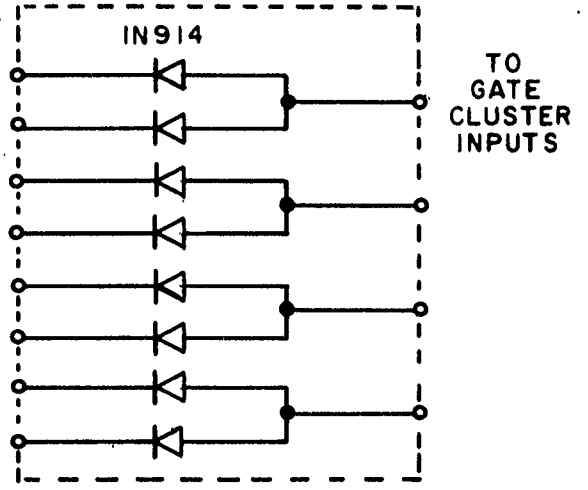


Figure 4-6. Diode cluster millimodule

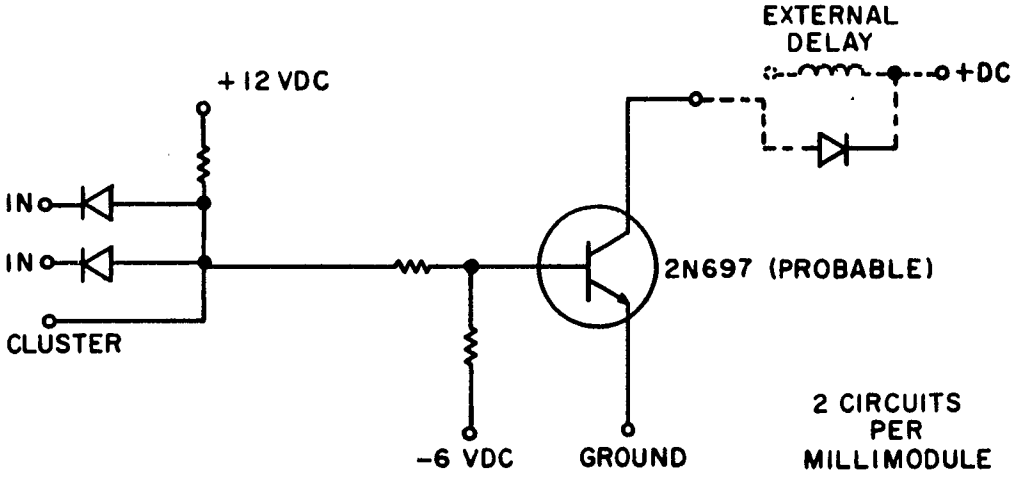


Figure 4-7. Relay driver millimodule-tentative circuit

4.1.5 PLANS FOR THE NEXT PERIOD

The nine types of standard millimodule circuits will be constructed in the final form factor, and design verification tests will be completed. Layout and drafting for these millimodules will be completed.

4.2 STANDARD PACKAGING DEVELOPMENT

Typical racks, chassis (stimuli and card type) and boards have been fabricated for a mechanical model. Figure 4-8 shows the complete assembly.

4.2.1 RACK

The rack height has been reduced to 66 inches in accordance with TDO MTE-1. Figure 4-9 shows the rack model with plenum and wiring frame installed.

4.2.2 DRAWERS

Figure 4-10 and 4-11 show typical MTE card and stimulus chassis. Some of the Simulated boards were removed from Figure 4-10 to show details of basket construction and printed board connectors. Figure 4-12 shows the rear of the card chassis with connectors in place. Preferred connector locations have been established and will be used throughout the system. A single connector is assigned for use with all ac and dc power inputs. Pin assignments within the power input connector has been made in accordance with ABMA STU-54C.

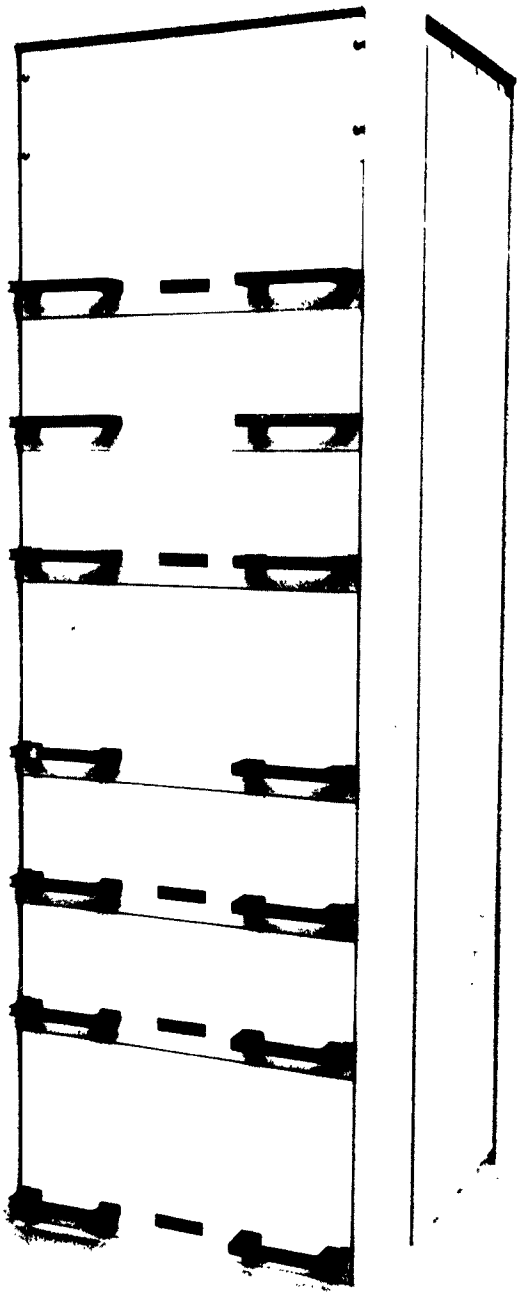


Figure 4-8. Typical rack

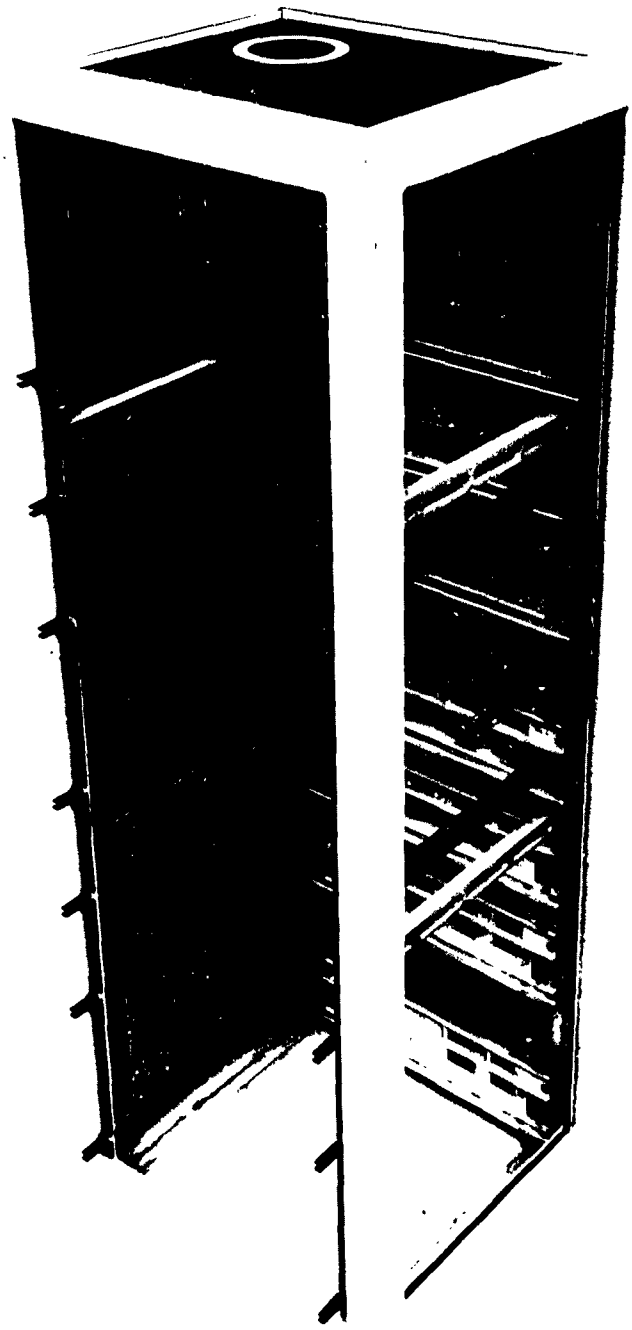


Figure 4-9. Typical rack-drawers removed

Figure 4-10. Typical card chassis

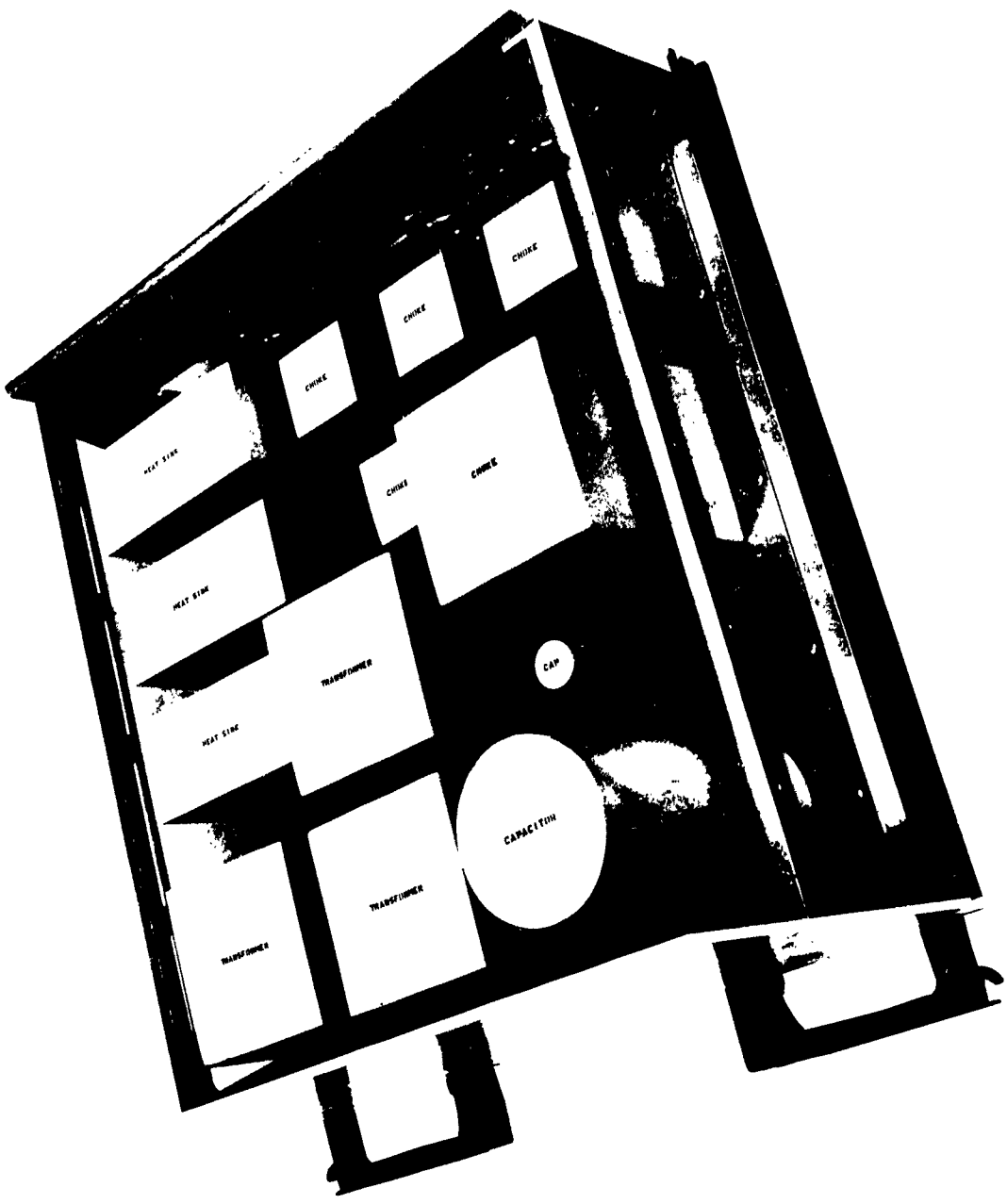


Figure 4-11. Typical stimulus chassis

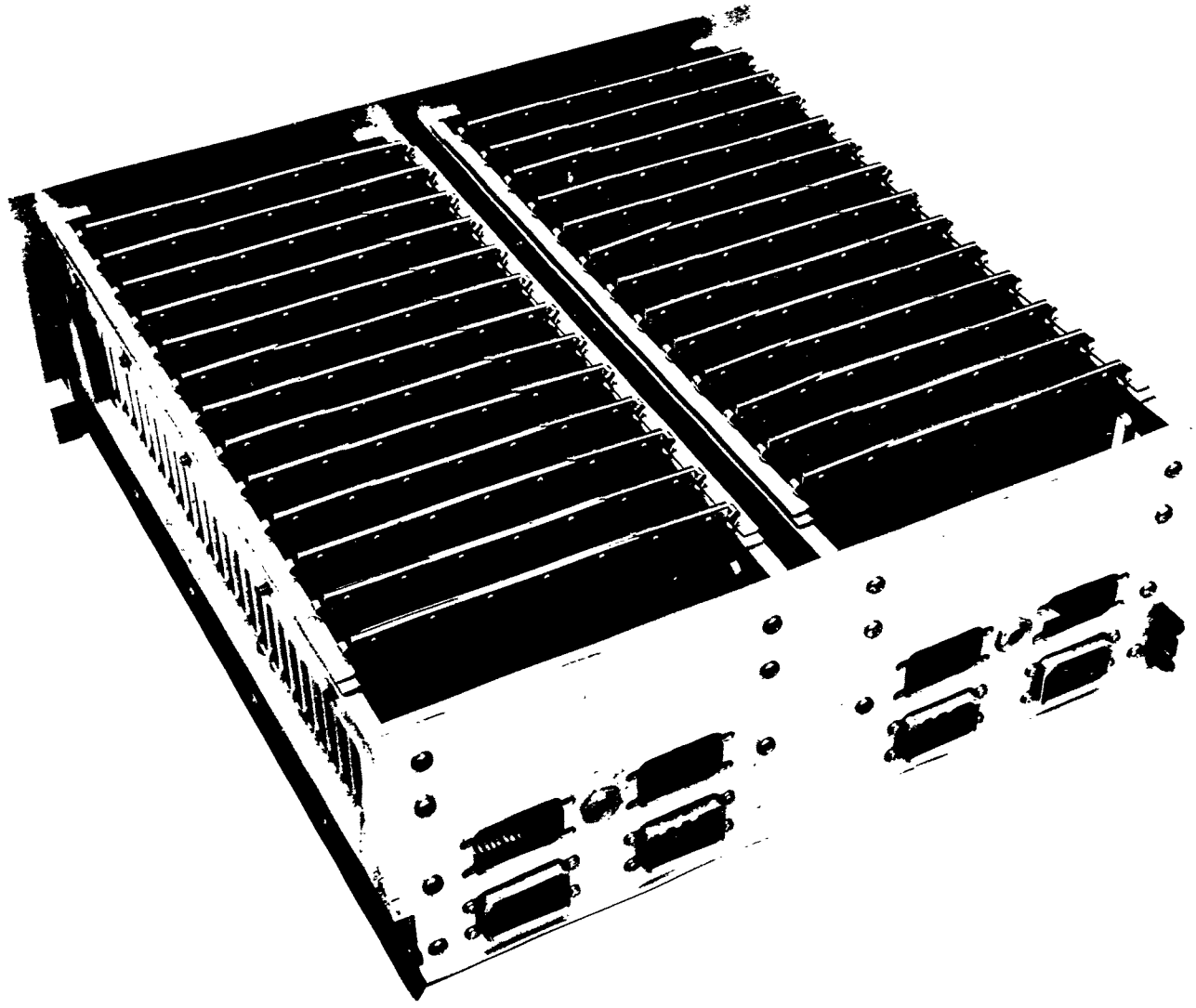


Figure 4-12. Chassis - rear view

SECTION 5

SHELTER DESIGN AND LAYOUT

5.1 SHELTER DESIGN

5.1.1 DESIGN OBJECTIVE

The design objective of this task is to house groups that compose a functional unit of MTE.

5.1.2 PROGRESS

Progress on the shelter design and layout task is reported under the following headings:

(1) General Equipment Arrangement and Configuration
(2) Shelter Work Surfaces Definition
(3) Shelter Lighting
(4) Shelter Weight Analysis
(5) Shelter Transportation.

5.1.3 GENERAL EQUIPMENT ARRANGEMENT AND CONFIGURATION

TDO-MTE-1 directed that a shelter of 87 inches maximum outside height be utilized for the Development Model MTE System.

In reply to TDO-MTE-1 an investigation was made into the apportionment of space within the RCA recommended shelter (See Vehicle and Shelter Study Report No. CR-62-547-6 dated 6 June 1962.) to redetermine the minimum shelter height to house the equipment.

Points considered are shown in Table 5-1. The total reduction in height is 6 inches, the originally recommended 85 inch inside height being reduced to a 79 inch inside height. This change represents the minimum shelter height that can be considered at this time.

Table 5-1. Shelter considerations.

Area Affected	Orig. 85" Inside	79" Inside
1. Air Conditioner return duct height	6"	4"
2. Rack height:	67 3/4"	66"
5840 Rack monitor panel	7"	5-1/4"
3. Rack connector availability:		
Top rack surface	Full width x full depth	Full width x 10" depth from front
Height for free access	5" over Full Area	6"
4. Air duct coupling to rack and Rack/Shelter mounting provisions	5"	2-3/4"
5. Console Height	67 3/4"	66"
6. Console Connector availability		
Top Console Surface	Full	Reduced- Must be shared with air duct coupling
7. Cooling Supply Duct Over Console	Unlimited	Duct cannot exist; must terminate at console
8. Test Stands, Storage Cabinets, etc. that must fit under cooling ducts	67 3/4"	66"

The reduction to a 4-inch high air return duct will effect an increase in air velocity and pressure drop.

The reduction of the rack height by 1 3/4 inches effects a compacting at the top level. The circuit breaker disconnect panel height will be decreased to 5 1/4 inches. Rack wiring to top connectors and air transition from rack top to plenum will now be limited to this reduced height allotment. The remaining electronic space allotment remains unchanged.

Decreasing the vertical distance between supply duct and rack top in effect reduces the available space for rack connectors by over 50%, limiting the number of connectors on this surface, and increasing the density of connectors along the front edge. Instead of a cabling trough running along the top rack surface, intercabling may have to be suspended from the shelter ceiling with connectors dropping down to racks. This will be considered when interrack wiring information is available.

The 2 3/4 inches between rack and supply duct is the practical minimum span necessary for flexible air duct/rack coupling, air metering to rack, and rack-to-shelter mounting provisions.

The reduction in console height and lowering of the console to the shorter return plenum, in conjunction with maintaining a fixed height work surface results in a nominal increase of 2 inches of rack surface on the lower section. The net result in the top section is to reduce the panel space by 3 3/4 inches. These changes will be adjusted to 1 3/4 and 3 1/2 inches on the standard panel increment basis. As the panel parameters become firm, a reallocation and reconfiguration of the control consoles will be in order

Due to the shallow depth of the upper section of the control consoles, the top surface must be shared by the connectors, the console supply duct coupling(s), and any supply duct requirements for the consoles. This reduction in shelter size imposes a possible termination of the air supply duct at the console to allow compatibility with console connector requirements.

The arrangements discussed above are compatible with the 87 inch outside shelter height directed by TDO-MTE-1, and resulted in an inside height of 79 inches. Craig will supply an S-141 type shelter to inside dimensions 79 inches high, 76 inches wide and 152 inches long, that falls within the maximum outside dimensions of 87 inches high, 83 1/2 inches wide and 163 inches long specified in the directive. This shelter has a basic weight of 1500 pounds and a payload capacity of 5000 pounds.

It is anticipated that the shelter dimensions called out in the Technical Direction Order will be adequate for the Service Test Models and beyond.

5.1.4 MTE WORK SURFACES DEFINITION

A. General

To develop work surfaces within MTE units, it is necessary to define their functions within each unit.

B. Electronic Test Unit 1 (ETU-1)

Table 5-2 defines the four ETU-1 work surfaces. These surfaces are referenced to position in the shelter by the equipment position key of Figure 5-1.

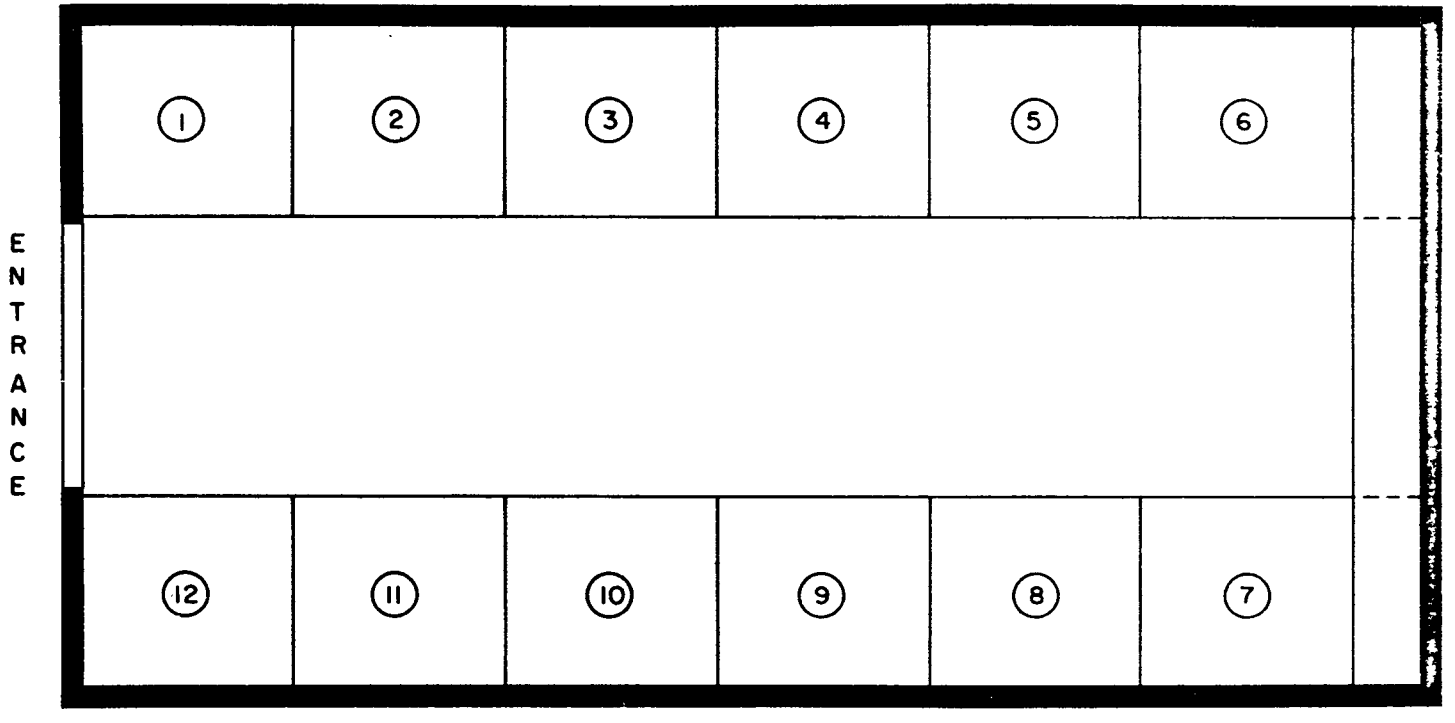


Figure 5-1. Shelter work surfaces - location key

a. Operator Control Console

This is the test control center for the Electronics Test Set. Small units will be tested on this surface which will also serve as a desk for the Electronic Test Set. The console counter top of insulating material must be physically able to support the weight of two men.

b. UUT Cooler

The top of the UUT cooler, at the normal 36 inch working height, will be a utility surface. Physically remote from other shop work areas, and associated with the UUT liquid cooling system, assembly and repair operations with possible liquid spillage should be limited to this surface. Provision is necessary for collection, storage and disposal of these liquids.

c. Primary Test Surface

This drop-leaf work surface is located between the Measurements Rack and High Frequency Stimulus No. 2 Racks, directly in front of the Monitor-Adapter panels. A UUT may be connected to the rack with minimum length adapter cables. This surface is so located that any UUT requiring coolant from the UUT cooler can be conveniently connected with flexible lines. The test surface will be electrically insulated, resistant to coolants and lubricants and equipped with a system ground connection. It will be capable of supporting the weight of two men. The test surface will be quickly detachable from either rack, the attaching hardware serving as a hinge, to swing surface down against the other rack for storage.

d. Disassembly/Repair Work Surface

Located directly across the aisle from the Operator Control Console, this surface will be used for the major portion of the disassembly,

reassembly and repair work of the Electronic Test Set. It will be hinged to fold up to expose the rate table which will be mounted on a floor stand.

C. Electronic Test Unit 2

No work surfaces are presently planned for this shelter.

D. Hydraulic Test Unit

A definition of the work areas is given in Table 5-3 and the equipment position key is as shown in Figure 5-1.

a. Operator Control Console

As in the Electronic Test Unit, this is the test control center; the bench requirements are identical.

b. Work Area (Position 4)

Located adjacent to the Control Console, this work surface will take pneumatic UUTs. Ready access to the controls (located underneath) will be provided, as well as an insulating surface and system ground.

c. Work Area (Position 7)

The work area surface forms the top of a half-height storage cabinet. It will support a man's weight and will be suitable for use both as a utility surface and as a disassembly and repair surface.

d. Work Area (Position 12)

This work surface also forms the top of a half-height storage cabinet. This surface is planned as the utility surface for hydraulic UUTs. Provision will be made for collecting and storing or disposing hydraulic fluids.

Table 5-2. ETU 1 work surface definitions

Position	Name	Nominal Size	Description
1 thru 3	Operator Control Console	48"x 17"	Work surface built into a console with racks of equipment above and below. Used as a desk, test surface and assembly surface. Has a kneehole for a stool.
6	UUT Cooler	24" x 22"	Top of a half rack containing the UUT Cooling system. Used for assembly, repair, and utility. This surface will be exposed to coolants and lubricants.
Between 4 and 9	Primary Test Surface (Drop-leaf)	24" x 32"	Removable work surface fastened between test equipment racks. May be unfastened on one side and swung down against the opposite rack. Used for test and some assembly. Most convenient for combined use of Control Console, Monitor Adapter connections and UUT Cooler, together with easy access to High Frequency Stimulus.
10 and 11	Disassembly and Repair Surface	48" x 22"	Folding work surface hinged to be raised to give access to the rate table. Used for disassembly, assembly, repair, and some testing. Has a kneehole for a stool.

Table 5-3. HTU work surfaces - definitions

Position	Name	Nominal Size	Description
1 thru 3	Operator Control Console	48" x 17"	Work surface built into a console with equipment above it and a kneehole below it. Used as a desk, test surface, and assembly surface.
4	Pneumatic Work Bench	24" x 22"	Continuation of Operator Control Console surface located on top of half high rack of pneumatic test gear. All pneumatic UUTs will be tested here.
7	Work Area	24" x 22"	Top of half-height storage cabinet. May be used as a utility surface and as a disassembly and repair surface.
9 thru 11	Hydraulic Test Stand	72"x 22"	Test surface built into the Hydraulic Test Stand. All Hydraulic UUTs will be tested within this unit
12	Work Area	24"x 22"	Top of half-height storage cabinet. This surface will be used as a utility surface for hydraulic UUTs and as such will be exposed to hydraulic fluids.

e. Hydraulic Test Stand

The built-in work surface will be capable of handling hydraulic fluids. Test connections will be built into the stand and the adjacent equipment rack so that all hydraulic tests may be performed here.

5.1.5 SHELTER LIGHTING

Lighting provisions planned are of two types: fixed or movable lights located above work surfaces and lights applied to the rack equipment areas. The former will not conflict with any shelter height considerations, but the latter must be positioned to illuminate the corridor between the racks as well as the front racks. For this second requirement, two approaches are possible: (1) sources mounted at the sides of the corridor, or (2) sources mounted centrally in this corridor. Side-mounting possibilities: (1) Cross aisle illumination which is subject to shadowing by the operator during use and the imposition of looking into the lighting source for the opposite rack illumination, and (2) shielded source on the same side as rack being illuminated for extreme glancing illumination.

The centrally-mounted corridor lighting which is shielded, eliminates the light source from direct view and still illuminates the rack fronts without cross light shadowing. This design can be implemented in 3 to 4 inches from the ceiling. Centrally-mounted lighting is recommended.

Head clearance with this shelter size is therefore, 75 to 76 inches in the equipment aisles, which is compatible with human factors design considerations. The crossover cable run to control consoles and cable entry panels, when short runs are necessary, will fall within this clearance.

No emergency lighting is required if no main power is available, as it is impossible to repair or test UUTs. The only need for lighting then would be to locate tools during intermittent shelter entry; the battle lantern provided with each shelter is probably sufficient for that purpose.

5.1.6 SHELTER WEIGHT ANALYSIS

A summary of MTE weight estimates are in the following tables.

Table 5-4. ETU 1 weight tabulation

ELECTRONICS TEST UNIT 1		
ITEM		WEIGHT pounds
Shelter Complement		2355
Equipment Complement		
Operator Control Console		919
Racks with Equipment		
Measurements	501	
Computer/Control	514	
Hi Freq Stimulus 1	487	
Hi Freq Stimulus 2	474	
Tape Transport	469	
Total	2445	2445
Storage Cabinet		375
UUT Liquid Cooler		150
Work Table and Tools		175
Work Table, Folding		50
Interrack Wiring		250
TOTAL WEIGHT ETU 1		6719

Table 5-5. ETU 2 weight tabulation

ELECTRONIC TEST UNIT 2

ITEM		WEIGHT(pounds)
Shelter Complement		2355
Equipment Complement		
Racks with Equipment		
DC Stimulus	853	
Internal P. S. 1	592	
Internal P. S. 2	487	
Storage Cabinet	375	
Low Freq Stim 1	712	
Low Freq Stim 2	610	
TOTAL	3629	3629
Interrack Wiring		175
External Cable Assys		400
TOTAL WEIGHT ETU 2		6559

Table 5-6. HTU weight tabulation

HYDRAULIC TEST UNIT

ITEM		WEIGHT (pounds)
Shelter Complement		2355
Equipment Complement		
Operator Control Console		746
Racks with Equipment		
Control and Stimulus	633	
Internal Power Supply	445	
Measurements	551	
TOTAL	1629	1629
Storage Cabinets (2)		440
Work Bench and Pneumatics		111
Tools		40
Hydraulic Test Stand		1100
Oil		200
Pneumatic Pump (Swingout)		45
Interrack Wiring		175
External Cable Assys		400
TOTAL WEIGHT HTU		7241

Table 5-7. Weight breakdown of major subassemblies

MTE SHELTER COMPLEMENT

Shelter (Basic)	1500 lb
Air Conditioners (2)	360
Air Conditioning Ducts	120
Rack Bases	200
Misc. Equipment	150
Lighting and Service Outlets	25
Total MTE Shelter Weight	2355 lb.

MTE RACK WEIGHT

Basic Rack		95 lb
Equipment Mounting Complement		
Air duct transition	0.6	
Plenum	6.2	
Connector panel frame	2.9	
	9.7	10
Electronic equipment rack		105
Level Mounting Complement		
Slide brackets	0.2	
Slides (1 pair)	4.0	
Connector Panel	1.8	
	6.0 lb/level	

STORAGE CABINETS

Basic Rack	95
Door and Shelves	30
Load	250
Total	375 lb

INTERRACK WIRING	35 lb/Rack

1/2 STORAGE CABINETS (HTU)

Cabinet	70
Load	150
	220 lb/Cabinet

CONTROL CONSOLES

ITEM	HYD-PNEU.	ELEC.
Left	150	150
Center	70	70
Right	70	100
Totals	290 lb	320 lb
Intrarack Wiring	60 lb	75 lb

UUT LIQUID COOLER

Cooler	100
Cabinet and Work Surface	50
TOTAL	150 lb

WORK TABLE AND TOOLS

Surface and Stool	50
Tools	100
Panel and Light	25
TOTAL	175 lb

EXTERNAL CABLE ASSY'S

Reel and Tie Downs	75
Cable Assy's	325
TOTAL	400 lb

WORKBENCH AND PNEUMATICS (HTU)

Work Bench and Storage Cabinet	75
Compressor Control	10
Accumulator	26
TOTAL	111 lb

5.1.7 SHELTER TRANSPORTATION

An envelope location of the shelter on the vehicles considered for this task is shown in Figures 5-2, 5-3, and 5-4. An approximate center of gravity for a typical shelter is indicated.

During the next quarter a center of gravity analysis of the loaded shelters will be made. A report on the handling of the shelters with Telefork 102 handling equipment will be prepared.

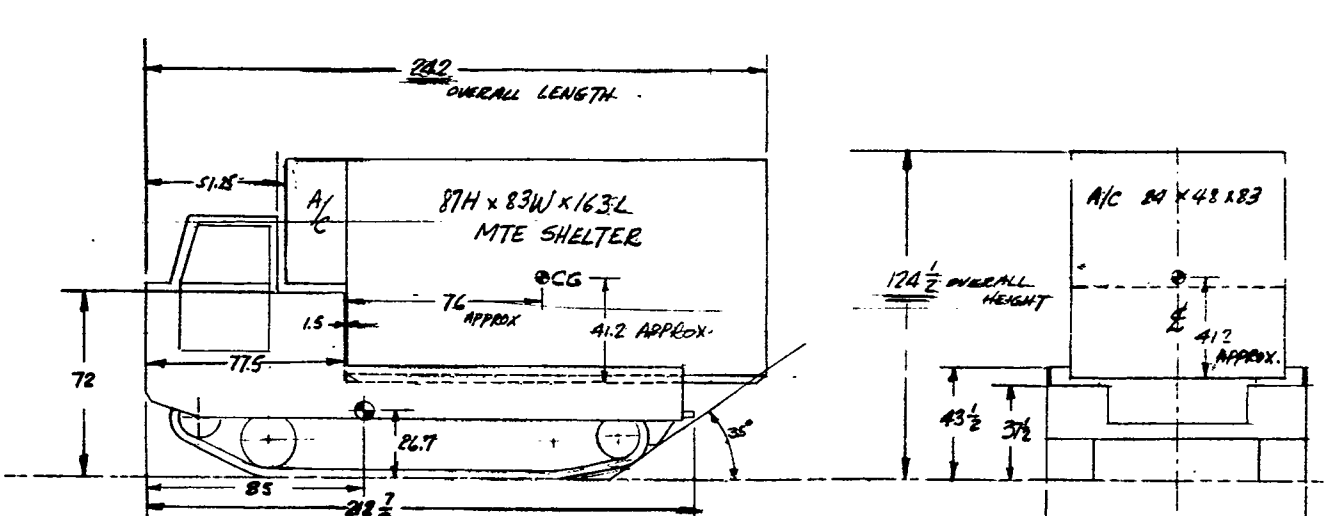


Figure 5-2. MTE shelter on XM-548

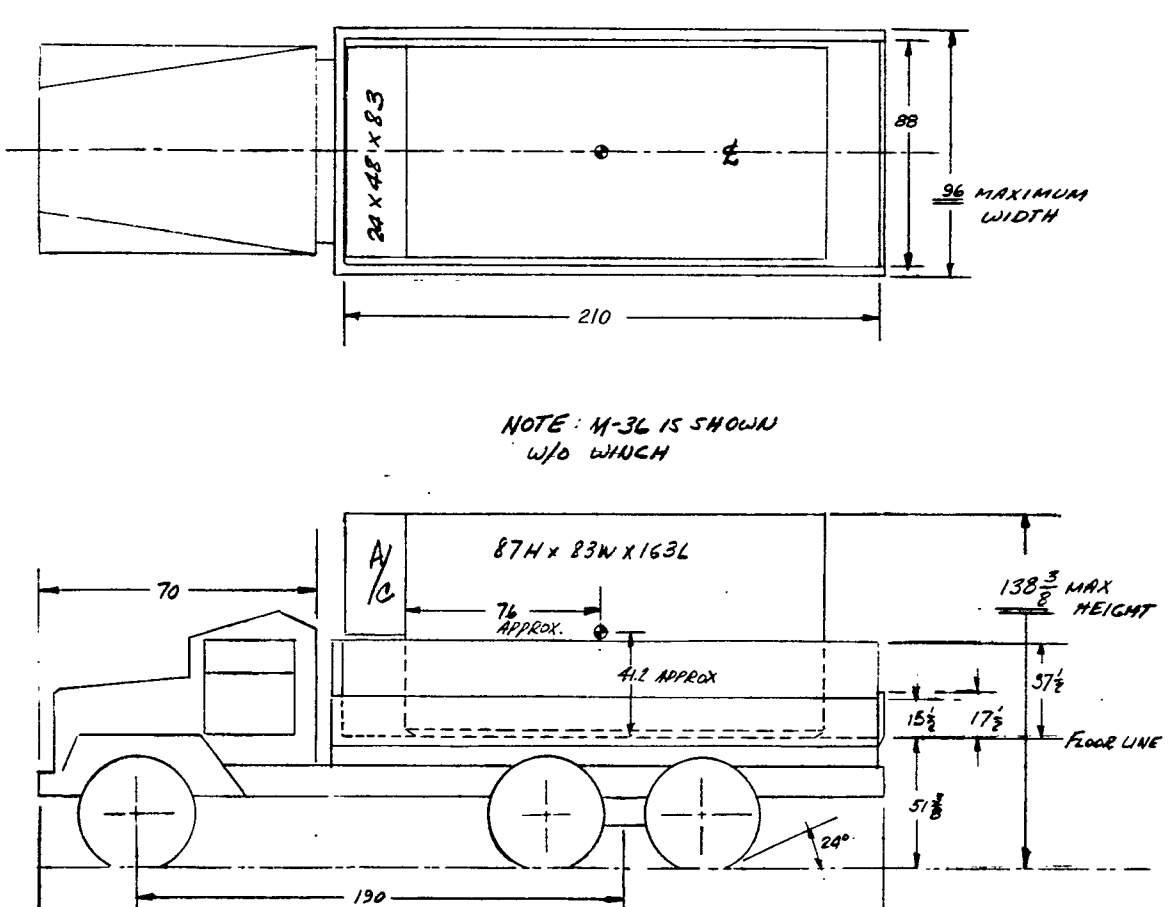


Figure 5-3. MTE shelter on M-36

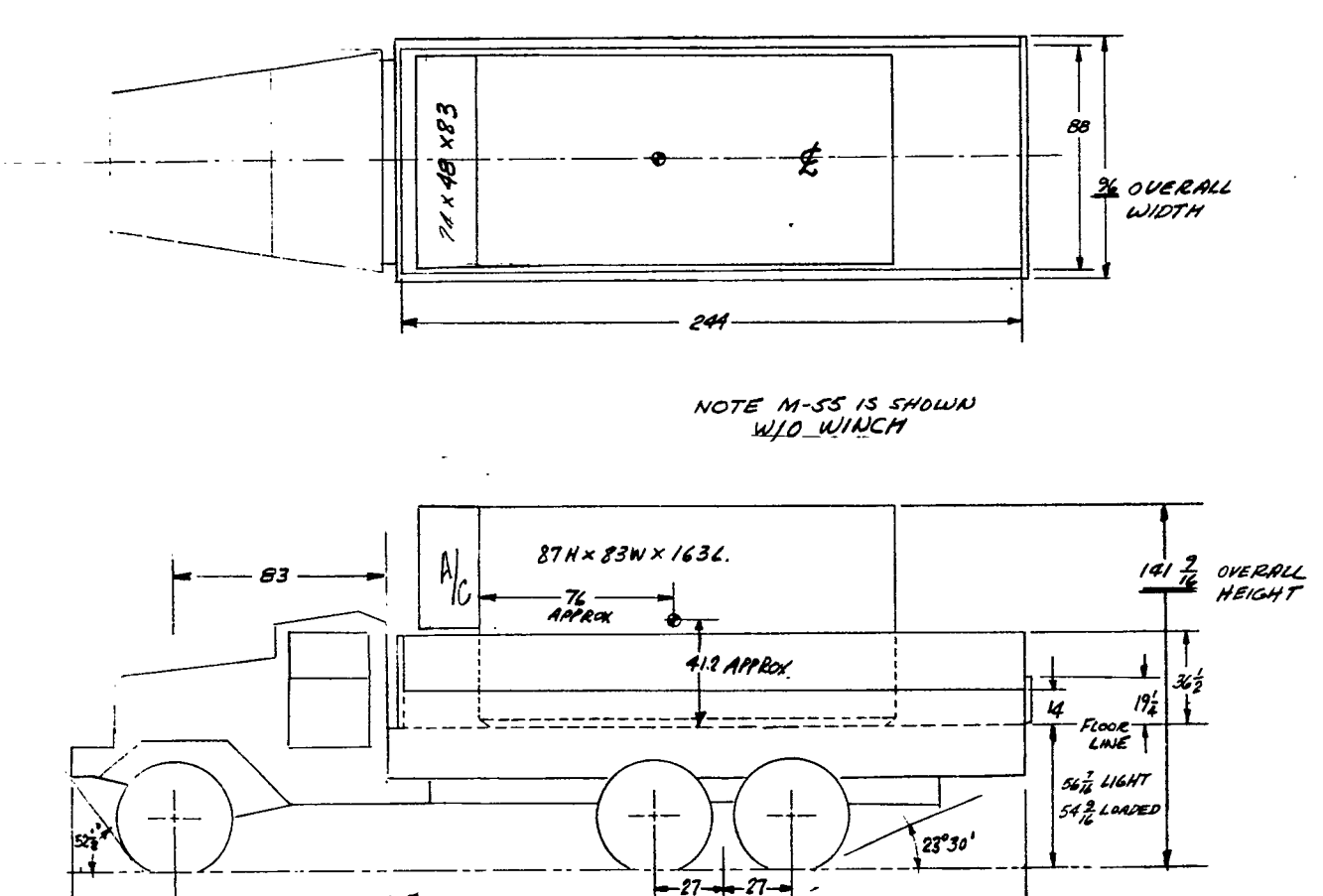


Figure 5-4. MTE shelter on M-55

5.2 SHELTER AND EQUIPMENT MOCKUPS

5.2.1 ONE-QUARTER SCALE MOCKUP

One set of four 1/4 scale shelter and equipment mockups has been built. This includes Electronic Test Unit 1, Electronic Test Unit 2, Hydraulic Test Unit and Pneumatic Test Unit. The Pneumatic Test Unit is included to show the four shelter concept.

The shelters include air conditioners, cable entries and external hook-up panels. The equipment complement is comprised of racks, consoles, test stands, work benches, storage cabinets and air conditioning ducts.

The mockups demonstrate equipment configuration, cooling methods and cabling distribution methods.

5.2.2 FULL SCALE MOCKUP

In order to illustrate and manipulate the equipment layout in the MTE shelter, a full-scale mockup of the ETU 1 has been constructed. This wooden mockup includes all racks, chassis, connectors, work areas, air conditioner mounting, cable entries, and lighting in an enclosure which conforms to the actual shelter dimensions.

5.2.3 PLANS FOR NEXT QUARTER

Both the full-scale and quarter-scale mockups will be used at the DCR on 15 and 16 January.

Full scale mockups of the ETU 2 and the HTU will be constructed.

5.3 HEATING, COOLING, AND VENTILATING DESIGN

5.3.1 GENERAL

This section describes progress in heating, cooling, and ventilating systems for shelter enclosures for Electronics Test Units 1 and 2, and the Hydraulic Test Unit.

A redetermination of the loads based on current equipment information is presented and analyzed; the thermal capacity of the CE20VAL4 air conditioner under various operating conditions is examined; and the application to a heating, cooling and ventilating system is developed.

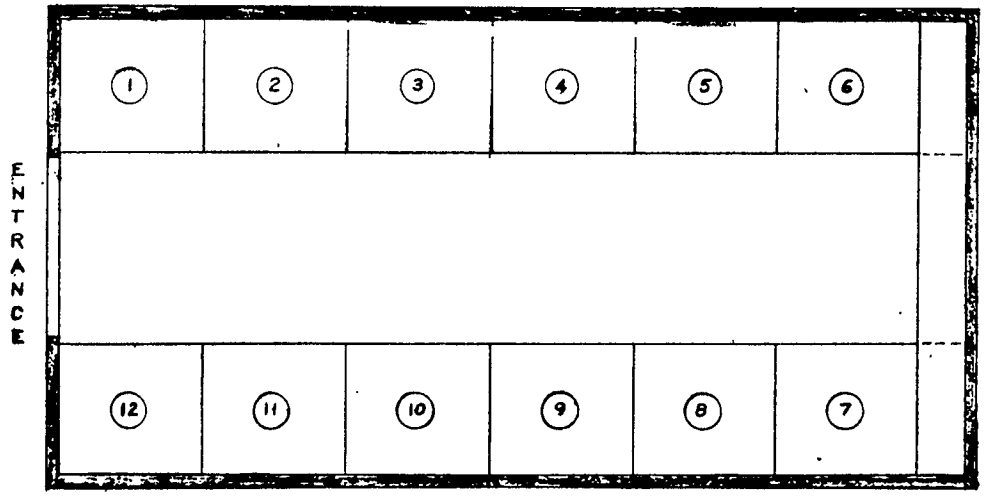
As a result of the initial investigation of this area, reported in the Air Conditioning Study Report CR62-547-5 (6 June 1962) an Air Conditioning unit was selected, as a basic building block that could be used in multiples of two or three for each shelter, to effectively handle the anticipated equipment, shelter, and personnel loads. The use of this unit was approved: Corps of Engineer Model CE20VAL4 Air Conditioner will be GFE for this task.

5.3.2 LOAD DETERMINATION

Thermal loads are impared within the shelter by the equipment and operating personnel. Equipment loads can be considered constant and independent of environment, but different with each shelter. Basic shelter loads are the same for each shelter but are dependent on the environmental differences across the interface. The number of operating personnel, and air infiltration through the shelter interface are dependent upon shelter equipment use.

Table 5-8. Heat load data-ETU 1

Location	Description of Source	Watts	Thermal Load BTU/HR
1 2 & 3	Operator Control Console	1910	6550
4	Measurements	530	1815
5	Computer/Controller	748	2560
6	UUT Coolers	350	1200
7	Storage	0	0
8	Hi Freq Stimulus No. 1	380	1300
9	Hi Freq Stimulus No. 2	250	850
10 & 11	Work Surface	20	682
12	Tape Transport	1797	6120
Total		5985	20500

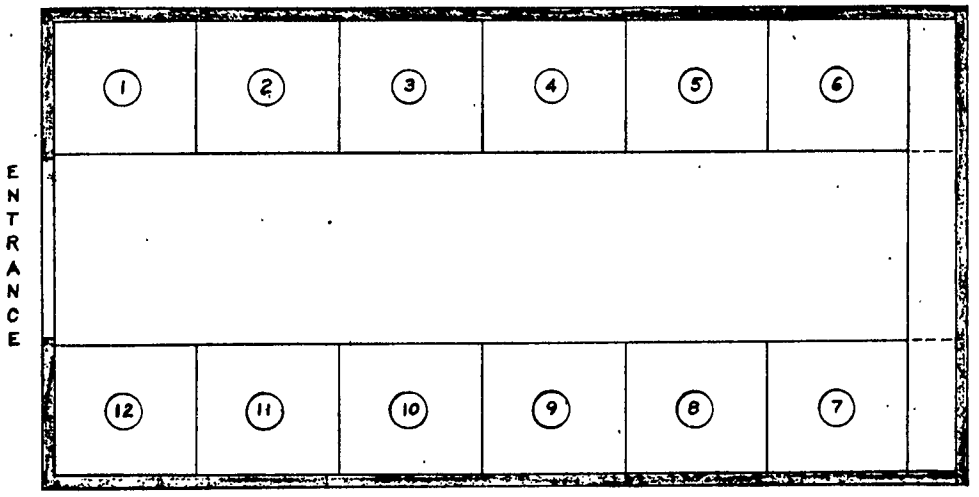


FLOOR PLAN

MTE SHELTER EQUIPMENT POSITION KEY

Table 5-9. Heat load data-ETU 2

Location	Description of Source	Watts	Thermal Load BTU/HR
1 & 2			
3	DC Stimulus	2530	8650
4	Int. Power Supply No. 1	425	1450
5	Int. Power Supply No. 2	340	1160
6 & 7			
8	Storage Cabinet	0	0
9	Low Freq Stimulus No. 1	1659	5650
10	Low Freq Stimulus No. 2	1214	4140
11 & 12			
Total		6168	21200

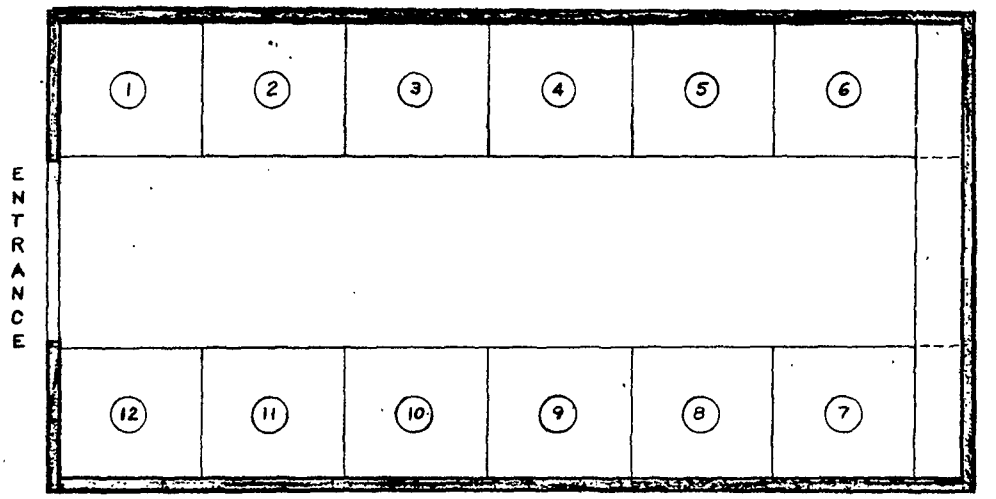


FLOOR PLAN

MTE SHELTER EQUIPMENT POSITION KEY

Table 5-10. Heat load data-HTU

Location	Description of Source	Watts	Thermal Load BTU/HR
2 & 3	Operation Control Console	1400	4790
4	Work Bench	111	380
5	Controller & Stimulus	1360	4650
6	Internal PS	275	940
7	Work area		
8	Measurements	924	3140
9 10 & 11	Hydraulic Test Stand	500	1710
12	Work Area		
Total		4569	15610



FLOOR PLAN

MTE SHELTER EQUIPMENT POSITION KEY

A. Equipment Loads

The equipment loads in the shelters result from the heat dissipation of electronic test equipment, electric motors, and pneumatic and hydraulic test equipment.

The sensible heat emanating from this equipment load is segragated, because it is a variable; most other sources of sensible heat remain fixed for each MTE shelter.

The summarized sensible heat load data for each shelter are shown in Tables 5-8, 5-9, and 5-10 with a plan view of each shelter locating each source of heat. The tables and charts, used for this load analysis, will be required later for air flow and control design.

B. Shelter Loads

The steady state shelter loads (independent of equipment) considered were: (1) shelter sensible heat loads; (2) shelter latent heat loads; and (3) shelter sensible heat loads. The loads were calculated for environmental conditions as shown in Table 5-11.

Table 5-11. Load calculations for various environmental conditions

Design Condition	Operation	Outside Design Conditions	Inside Design Conditions
No. 1	Worldwide Hot	125°F db, 13 gr/ft^3	90° db 50% RH
No. 2	Worldwide Hot	110°F db, 13 gr/ft^3	90° db 50% RH
No. 3	Worldwide Tropics	95°F db, 13 gr/ft^3	90° db 50% RH
No. 4	Worldwide Hot	90°F db, 13 gr/ft^3	90° db 50% RH
No. 5	Desert	125°F db, 1/2 gr/ft^3	90° db 50% RH
No. 6	Worldwide Wet	85°F db, 13 gr/ft^3	90° db 50% RH
No. 7	Worldwide Wet	80°F db, 100% RH	90° db 50% RH
No. 8	Arctic	-65°F db, 100% RH	50° db 50% RH

a. Shelter Sensible and Latent Heat Loads

The shelter sensible heat arises from conduction through shelter walls, human occupants, ventilation air, and shelter lighting equipment.

The sources of latent heat are personnel, ventilation air, and infiltration air.

Design condition # 1, applied to ETU-1 and HTU assumes:

> 85^{o} dew point, 0.55 BTU/hr/sq ft heat transfer coefficient, and 1000 watts of lighting; two people in shelter each require 10 ctm of fresh air; door opened once each five minutes admits 100 cu ft of air.

Heat loads are calculated as shown in Table 5-12.

Table 5-12. Calculated heat loads

	Sensible Load BTU/hr	Latent Load BTU/hr
Roof	5115	
Sidewalls	6600	
Floor	1545	
People	440	560
Ventilation Air	760	1090
Infiltration through door	760	1090
Lighting	3415	
	18635	2740

As ETU-2 is normally unattended, only two door openings per hour with resultant infiltration air were considered. A minimum of 20 cfm of fresh air will be brought in through the air conditioners. The sensible heat load will be 18635-440 $\cong$ 18200 BTU/hr, and the latent heat load will be 2740-560 = 2180 BTU/hr.

b. Shelter

Heating the shelter minimum load was found to be -30913 BTU/hr. The negative sign indicates that heat, rather than cooling, must be supplied to maintain the shelter under equilibrium condition.

c. Summary

Cooling/Warning Loads, All Design Conditions tabulated results of the calculations for shelter sensible and latent heat loads for design conditions 1 through 8 are shown in Table 5-14.

C. Total Unit Thermal Loads

The summation of the equipment and shelter loads are presented in Table 5-13, considering each unit under the most severe steady state cooling or heating conditions.

Table 5-13 Total unit thermal loads

	BTU/hr ETU1	BTU/hr ETU2	BTU/hr HTU
Equipment Sensible Heat Loads	20500	21200	15610
Shelter Max SH	18635	15149	18635
" " LH	2740	2180	2740
Shelter Min SH	30469	30913	30469
" " LH	560		560
Total Unit Max	41875	38529	36985
SHR	0.935	0.945	0.93
Total Unit Min	-9409	-9713	-14299

Table 5-14 Shelter sensible and latent heat loads

Design Cond	SHELTER SENSIBLE BTU/HR			SHELTER LATENT BTU/HR			TOTAL SHELTER LOAD BTU/HR		
	ETU1	ETU2	HTU	ETU1	ETU2	HTU	ETU1	ETU2	HPTU
1	18635	15149	18635	2740	2180	2740	21375	17329	21375
2	14587	10732	14587	2740	2180	2740	17327	12912	17327
3	10591	6736	10591	2740	2180	2740	13330	8916	13330
4	9245	5385	9245	2740	2180	2740	11985	7565	11985
5	18641	14786	18641	-2272	-2832	-2272	16369	11954	16369
6	8315	4460	8315	2740	2180	2740	11055	6640	11055
7	7405	3550	7405	2740	2180	2740	10145	5730	10145
8	-30469	-30913	-30469	500		560	-29909	-30913	-29909

5.3.3 CAPACITY DETERMINATION OF TRANE AIR CONDITIONING UNIT CE20VAL4

The performance data of this unit is given in Corps of Engineers Publication, 7610-C-1-224, Manual for Air Conditioner, Self Contained, Model CE20VAL4. Its major characteristics are:

Cooling Capacity	18000 BTU/HR Nominal 19800 BTU/HR Actual at 125° FDB air to condenser 90° FDB to unit at 1.0 specific Heat Ratio
Heating Capacity	12000 BTU/HR High Heat 6000 BTU/HR Low Heat
Approximate Weight	180 lb

From a capacity evaluation point of view, the given performance data is of limited value since capacity varies considerably with different SHR (Specific Heat Ratio) values. The data in Table 5-15 for CE20VAL4 unit is taken from "Lightweight Military Air Conditioners, Preliminary Specifications," published by U.S. Army Engineer Research and Development laboratories, Corps of Engineers, Fort Belvoir, Virginia.

Table 5-15. Performance data for the CE20VAL4

Outside Air Temp. Entering Condenser		Dry Bulb Temp Entering Unit								
		70°			80°			90°		
		Wet Bulb Temperature Entering Unit								
		55	59	63	59	63	67	61	71	75
95	BTU/hr	19600	20400	21200	20600	21200	22000	22000	22800	23600
	SHR	0.91	0.74	0.56	1.0	0.87	0.70	0.95	0.80	0.66
125	BTU/hr	17400	18200	19000	18600	19000	19800	19800	20000	21400
	SHR	0.97	0.79	0.60	1.0	0.92	0.75	1.0	0.85	0.70

This information is presented in graphical form (see Figure 5-5) to facilitate thermodynamic analysis.

5.3.4 NUMBER OF AIR CONDITIONER UNITS REQUIRED

Considering the maximum air conditioning load conditions above, an analasis was made to determine the number of air conditioner units to be used per shelter.

By psychrometric analysis, the air dry bulb temperature was found to be 90.8°F db, and the corresponding wet bulb temperature was 75.5°F WB. From Figure 5-5 , the capacity and SHR values were interpolated as 21600 BTU/hr and 0.69, respectively.

Therefore with the air conditioner operating on return air of 90°F db and 75°F WB, it has sensible heat capacity of only 14900 BTU/hr, and latent heat capacity of 6700 BTU/hr. For this condition, latent heat capacity greatly exceeds latent heat load.

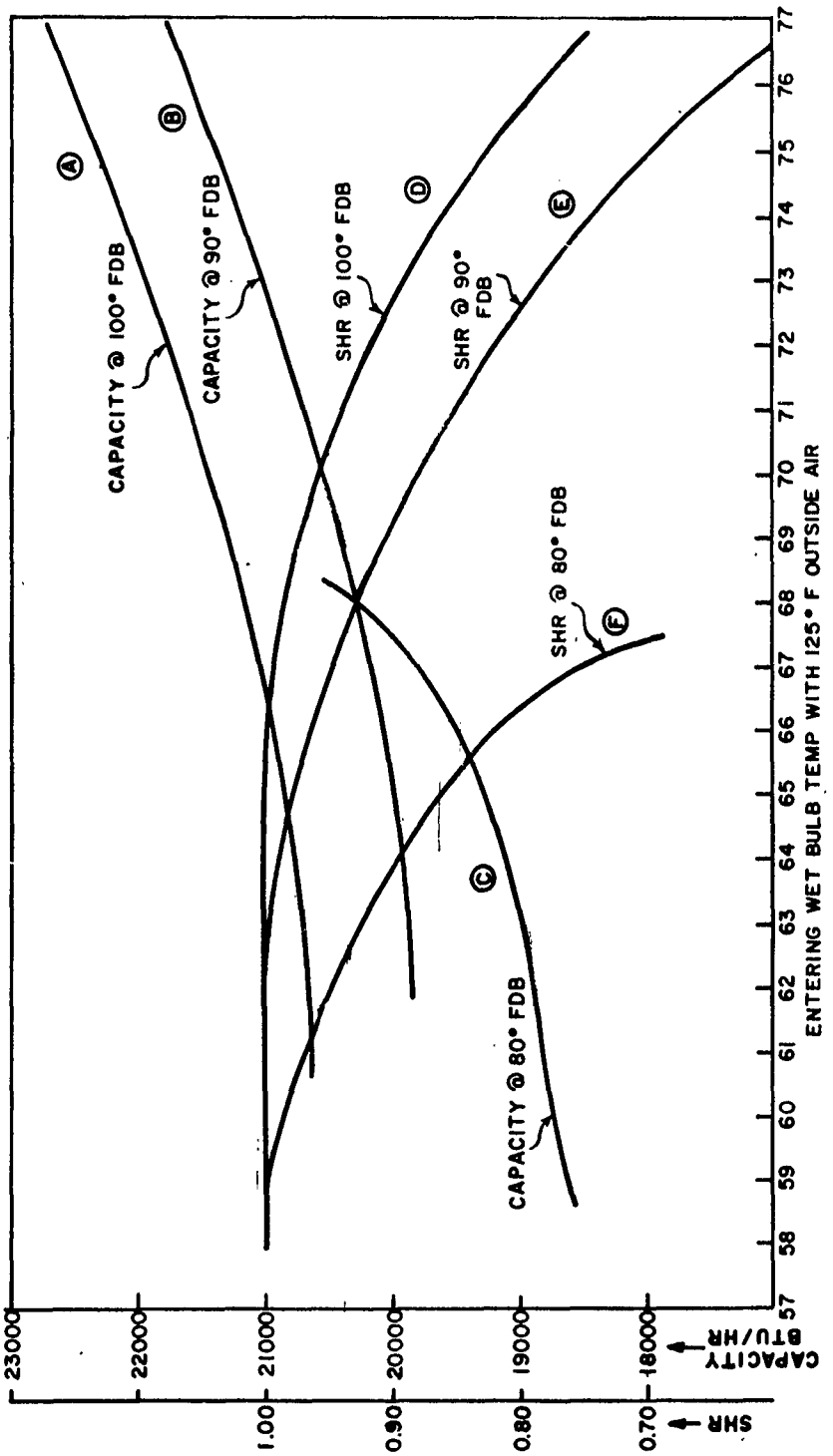


Figure 5-5. Characteristics - CE20VAL4 air conditioner

From a total capacity viewpoint (under the maximum hot, humid world-wide conditions) the maximum steady state unit load of 41875 BTU/hr can be handled by two air conditioning units.

Considering the available sensible capacity only, under the desired return air conditions, two units could handle only 29800 BTU/hr of the 39135 BTU/hr sensible load; ultimate equilibrium temperature within the shelter would then be approximately

$$90^{\circ}F \text{ db} + \frac{9704}{1280 \text{ CFM} \times 1.085} = 97^{\circ}F \text{ db.}$$

Actually the loads would decrease slightly, resulting in a slight reduction of this temperature.

The excess latent capacity will also affect the equilibrium wet bulb temperature also. The wet bulb temperature will decrease, reducing the relative humidity below the desired 50 percent point and increasing the latent loads that must be handled; this will permit an increase in the sensible heat capacity of the unit. To illustrate, if the design conditioner were $90^{\circ}F$ db, $68^{\circ}F$ WB the capcity of the air conditioner would be 20, 500 BTU/hr with a 5 h r of 0.92. This represents a sensible heat capacity of 18850 BTU/hr and a latent heat capacity of 1650 BTU/hr. The maximum steady state unit load, under this condition is 39004 BTU/hr sensible and 3720 BTU/hr latent with a specific heat ratio of 0.915. This design condition almost represents the equilibrium condition, in that two air conditioning units have a capacity of 37700 BTU/hr sensible heat and 3300 BTU/hr latent heat. The mismatch of the equilibrium point that still exists in the latent capacity will cause a slight increase in the wet bulb temperature. The mismatch in the sensible heat capacity will result in a dry bulb temperature slightly less then

$$90^{\circ}F \text{ db} + \frac{1304}{1280 \times 1.085} = 91^{\circ}F.$$

The accuracy of this analysis exceeds the accuracy of the estimated equipment loads and assumptions. Continual monitoring and reevaluation during the program may alter these figures. Based on present information, it may be concluded that two air conditioners per shelter are sufficient if a small increase in temperature can be tolerated; if the temperature increase cannot be tolerated, three air conditioners will be required. One air conditioner weighs 180 pounds, requires 6.6 kw in addition to the cost of the unit.

Considering the minimum load requirements, where heat must be added to maintain the unit within equilibrium design conditions, the use of two air conditioners (each with 12000 BTU/hr heating capacity) will handle the - 14, 299 BTU/hr load.

5.3.5 PLANS FOR THE NEXT INTERVAL

Analysis will be continued of the distribution system, pressure drops, possible use of booster fans with the increase in system complexity, load and noise. The net effect revealed by the analysis on the final number of air conditioning units will be presented.

SECTION 6

EQUIPMENT DEVELOPMENT

6.1 EQUIPMENT DEVELOPMENT - ELECTRONIC TEST UNIT (ETU)

6.1.1 COMPUTER/CONTROLLER GROUP

A. Progress During Quarter

Computer/Controller design was completed during the quarter and is described in detail in Appendix A. Major development effort during the quarter was concerned with the following:

(1) Vendors were contacted for long-lead items. Specifications and requests for quote have been sent to a number of vendors for paper tape readers, paper tape punches, magnetic tape transports, keyboards, printers and visual instructors (microfilm readers).

(2) Material and hardware were released for fabrication of Computer/Controller chassis. Bulk materials were released for fabrication of Controller millimodules (standard circuits).

(3) Computer A building block packaging concept was developed for the modified AM-3220 (silicon version of AM-3100) Computer. Logical division of computer circuitry and functions will result in a design with the following building blocks packaged to MTE standards:

Arithmetic Unit	MTE-5811
Control	MTE-5836
Memory	MTE-5837
Input/Output Buffer	MTE-5809

(4) Controller Preliminary logic designs have been completed for the Digital Comparator and Tape Search and Control. Logic design has been started for the Input/Output Buffer, Control, Printer Control, Punch Control and Tape Reader Control.

(5) System Switching language development has been started. This effort will define control requirements and word structure for all stimuli and measurement functions.

B. Plans for the Next Period

(1) Complete the detailed logic design of the Controller

(2) Release to manufacturing the bulk material for computer modules

(3) Prepare detailed MTE switching and control diagram, showing overall system signal and control data flow

(4) Place purchase orders for peripheral equipment contingent upon Government approval of recommended vendors

(5) Begin release of building blocks for fabrication and assembly of the Controller

(6) Begin effort on Computer/Controller test plans and test procedures

(7) Begin preparation of preliminary programming manuals for the Electronic Test Units and Hydraulic Test Unit.

6.1.2 HIGH FREQUENCY STIMULUS

During the present quarter the High Frequency Stimulus overall block diagram was prepared on an assembly-by-assembly basis (see Figure 6-1); progress on each of the fourteen assemblies is now reported individually (Sections 6.1 2.A through 6.1.2,1.N below)

Also during this quarter, a new arrangement was developed for the High Frequency Stimulus units as installed in the two equipment racks; mechanical design information is given in Section 6.1.2.0 below.

YIG filter development is described in paragraph 6.1.2.P.

A. 300-399 Mc Frequency Synthesizer

A simplified block diagram of the 300-299 Mc Frequency Synthesizer is snown in Figure 6-2

a 28-37 Mc and 20-29 Mc Interpolators

The 28-37 Mc and 20-29 Mc interpolator oscillator loops and their associated amplifiers have been tested Some work remains to be done in terms of temperature compensation of the varactor tuning element. For a temperature increase of 50°C an average increase of inductance and capacitance has been measured to be +250 ppm for every degree centigrade temperature rise Compensation is to be achieved with the application of INVAR magnet wire and series capacitors of a negative temperature characteristic, this will be accomplished during the next quarter. Both interpolator loops and the three associated amplifiers are ready for packaging; this will be completed during the next quarter The pulse lock technique, which is employed in the oscillators, has proven to be reliable and produces very few unwanted outputs. Without special filters the spurious outputs are approximately 40 db

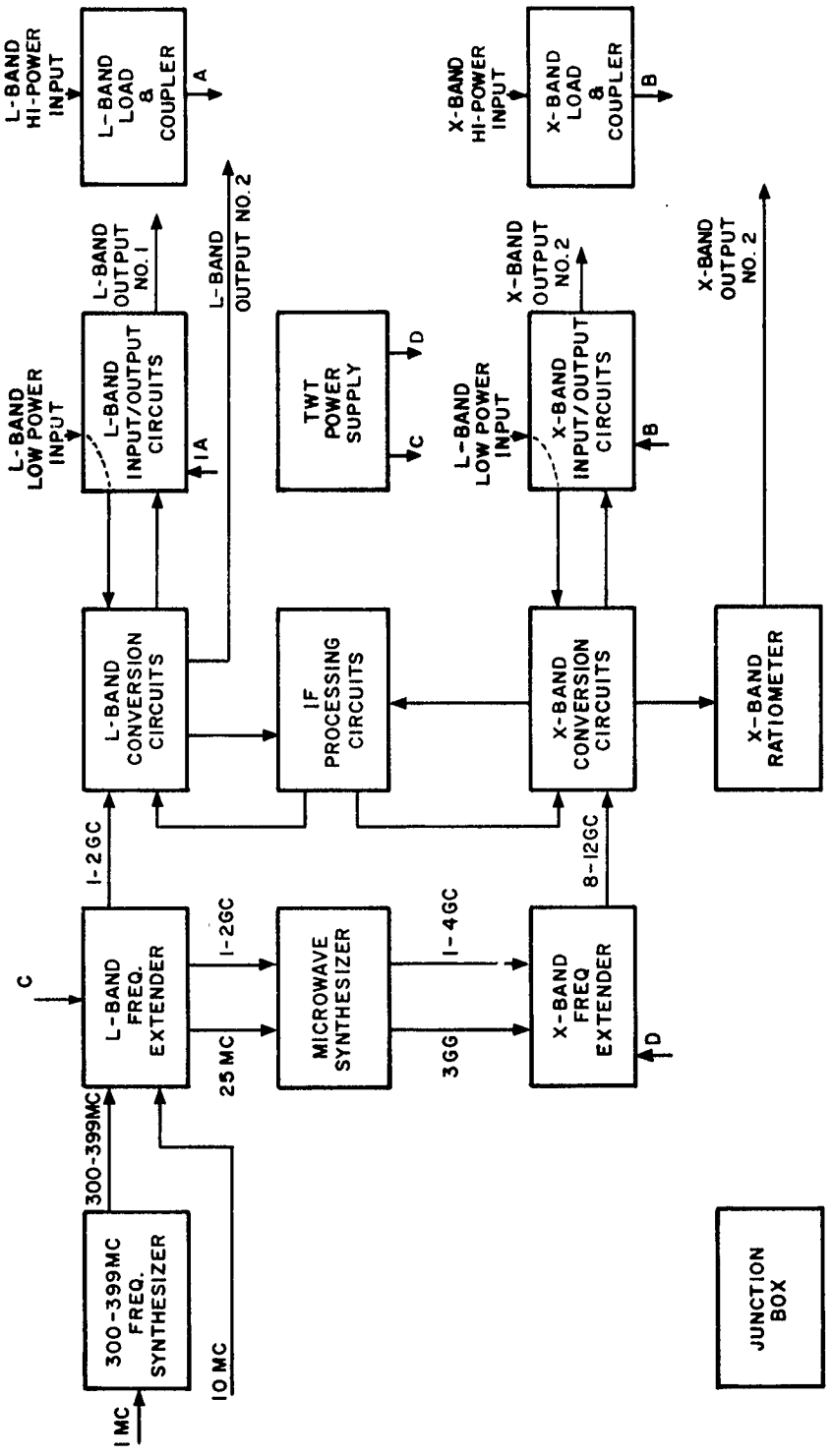


Figure 6-1 High frequency stimulus - simplified block diagram

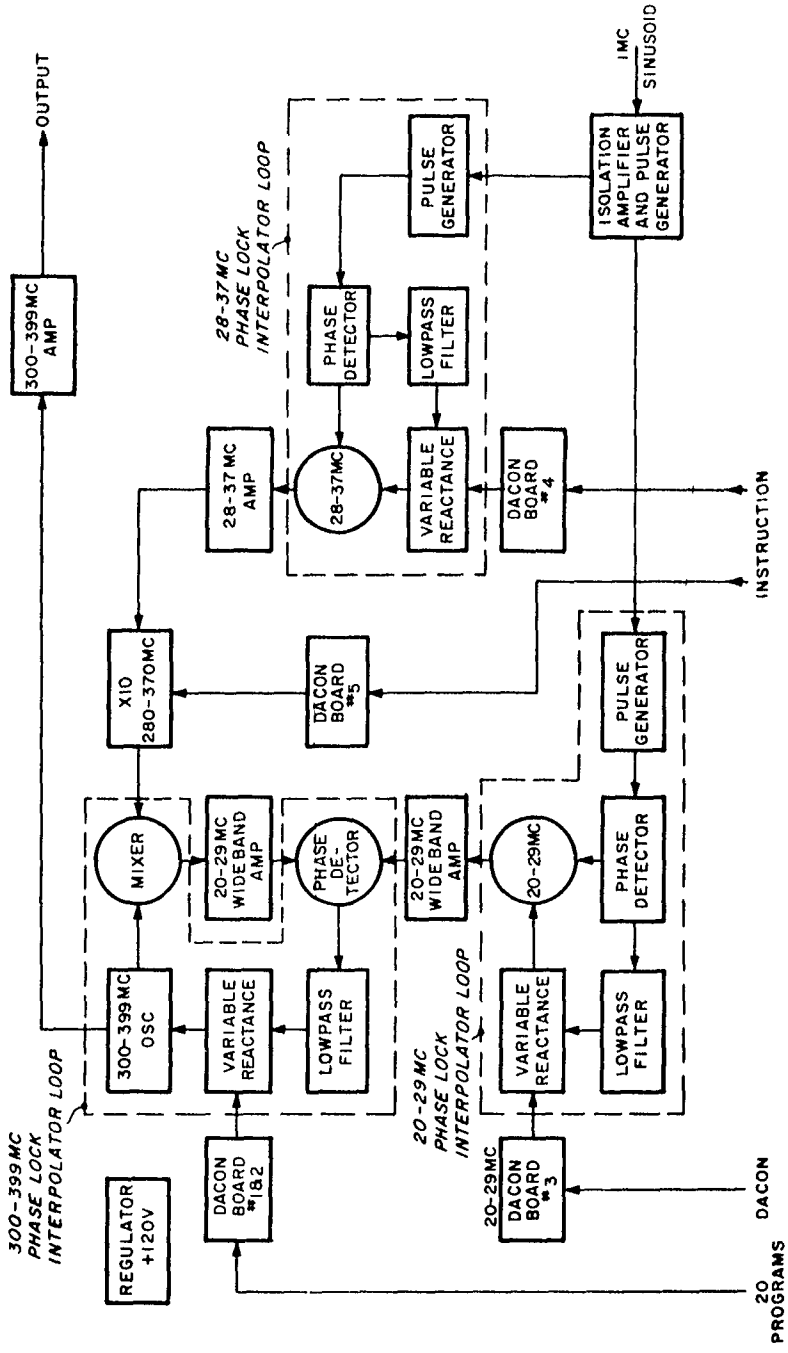


Figure 6-2. 300-399 Mc frequency synthesizer - block diagram

below the desired output frequency, this is an acceptable value The capture range is ±50 kc at 37 Mc and ±100 kc at 28 Mc. The attained capture ranges are adequate for the system, and measurements show that the holding range is approximately 5 times the capture range

b x10 Multiplier

Use of varactors for the x10 multiplier has been discarded because the characteristic Q of a varactor diode falls below a figure acceptable for the development of the design objective A step recovery diode is now being evaluated for this multiplier; because of the abrupt recovery function in the reverse conductive mode of a step recovery diode, a harmonic generator of high order harmonics is possible. The 10th harmonic will be filtered out by a tracking filter composed of three varactor tuned stages, calculated to reject the 9th and 11th harmonics to 40 db below the output of the 10th harmonic. A special wideband amplifier from 280 to 370 Mc will amplify the signal to a level compatible for the mixer in the 300-399 Mc oscillator loop. The x10 multiplier is in the breadboard stage, and considerable design effort and emphasis on the tracking filter is required. This effort will be completed during the next quater, and the multiplier will be released for packaging.

c 300-399 Mc Interpolator

A number of design areas will be investigated before the development of the 300-399 Mc loop.

It is planned that the oscillator will be programmed in 5-Mc increments By doing so, frequency error discrimination is eased, which in the worst case could be no more than 2 Mc away from the reference carrier which is generated in the 20-29 Mc interpolator loop

Temperature runs on the oscillator from 22°C to 70°C indicated a frequency variation of 970 kc when the output frequency was set at 300.06 Mc, and 3.1 Mc when the output frequency was set at 394.7 Mc. These variations are approximately 0.3 % and 0.9 %. Additional breadboard testing during the next quarter should lead to a final design.

Mixer circuitry is being evaluated. It is intended to employ wideband balun type transformers to feed the two high frequency carriers to a balanced mixer in order to suppress the input comirs; various types of mixers will be evaluated, including a transistor mixer. Breadboard construction and test should be completed during the next quater.

The variable reactance, low pass filter and phase detector will be designed, breadboarded and tested during the next quarter.

Effort will be made during the next quarter to finalize circuitry, complete breadboard construction and evaluation, and release the 300-399 Mc Interpolater for mechanical packaging.

d. Data Conversion

Data conversion basic circuits were designed, tested, and nearly all released to manufacturing. Values must be defined for each of the potentiometers which are in the ten output lines. Complete release to manufacturing will be accomplished during the next quarter.

e. Voltage Regulator

The voltage regulator was designed, breadboarded and evaluated. Additional design effort is required to meet the objective of 0.01 % stability.

Negative temperature coefficient references may be provided in the feedback loop to offset the inherent temperature coefficients of the tuning elements of oscillators and the increase in current gain in the transistors used in the oscillators.

The voltage regulator will be released to manufacturing during the next quarter.

f. Isolation Amplifier and Pulse Generator

A circuit was designed and breadboarded. Evaluation started during this quarter will be completed and the unit released for mechanical packaging.

B. L-Band Frequency Extender

A block diagram of the L-Band Frequency Extender is shown in Figure 6-3.

a. Multipliers

Design work on the multipliers (see Figure 6-3) began during the quarter. A 10 Mc sine wave will be available at the input, instead of the 1 Mc square wave as reported previously. This simplifies the design, since 10-Mc sidebands are more easily filtered than 1-Mc sidebands. All multiplier circuits were designed, and construction of breadboards started. The x2.5 circuit indicated in Figure 6-3 is actually an x5 circuit followed by a divide by two circuit.

During the next quarter construction of breadboards and performance evaluation will be completed; the multipliers will be released to drafting.

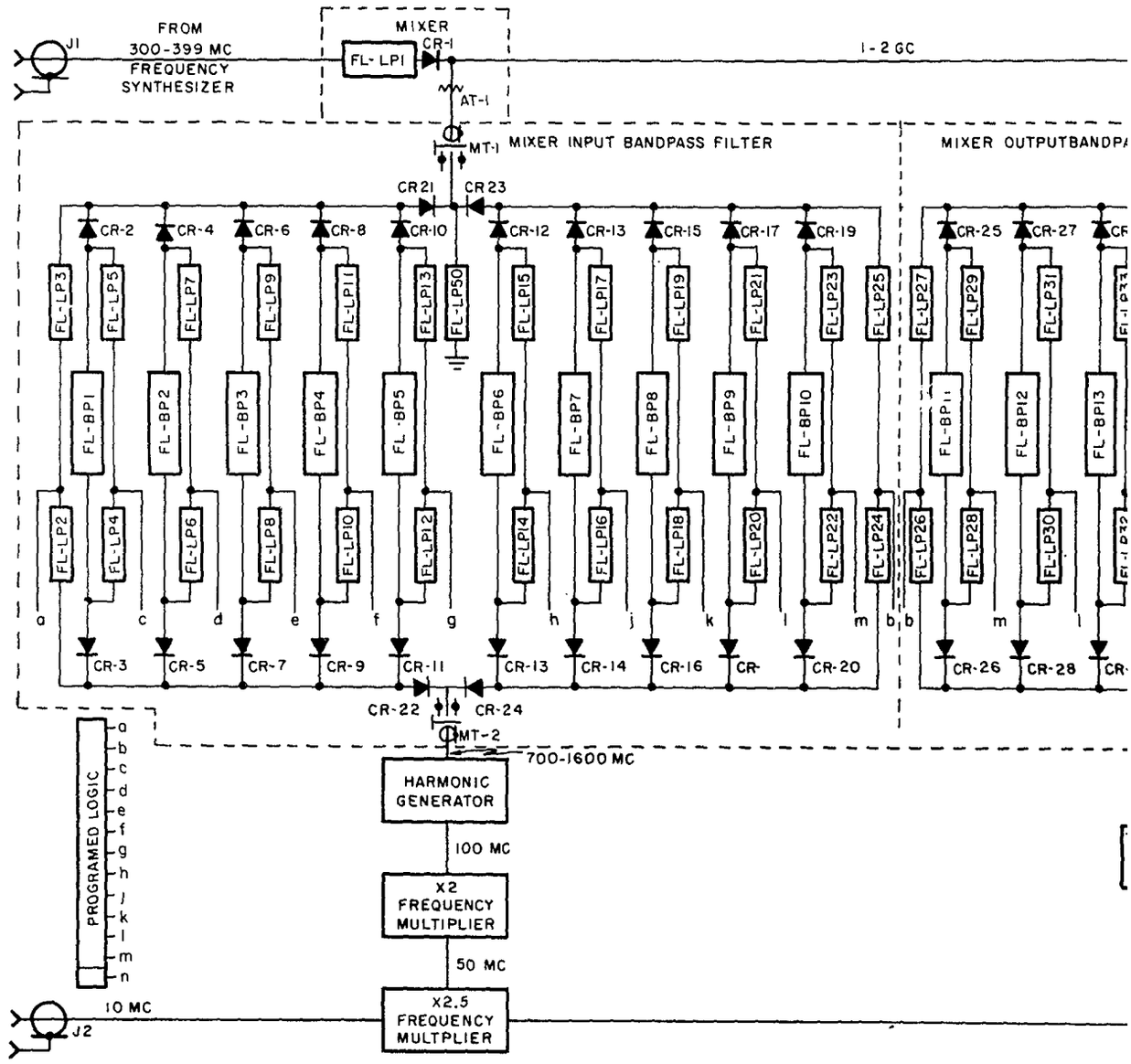


Figure 6-3. L-band frequency extender -

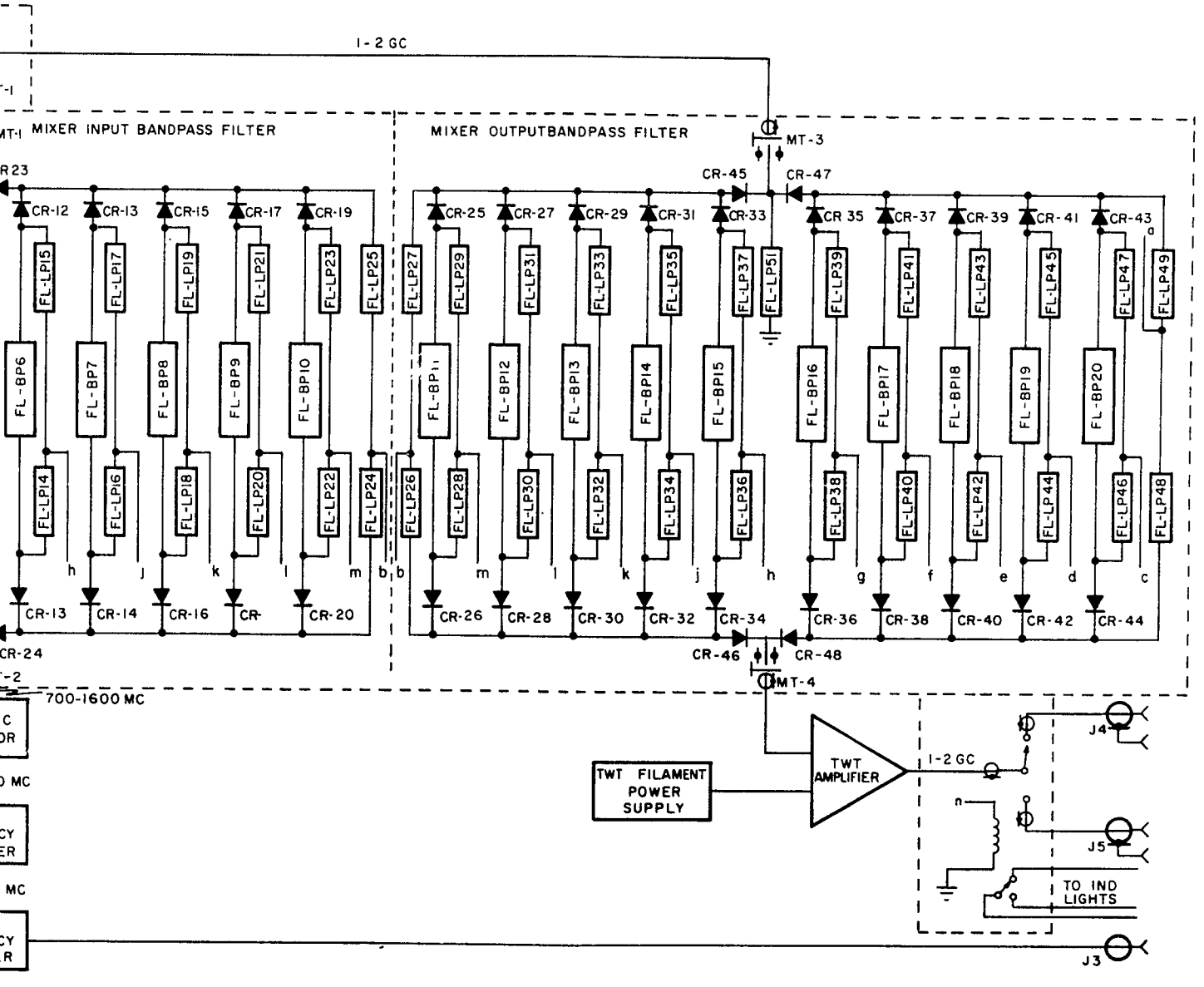


Figure 6-3. L-band frequency extender - block diagram

b. Harmonic Generator

The circuit developed during the quarter uses a step recovery diode as the harmonic generating element. The untuned output is fed to a bank of bandpass filters which act as tuned loads for the 7th through 16th harmonics of the 100-Mc input signal.

During the next quarter, a breadboard will be constructed and tested. In the event of insufficient harmonic output, a separate harmonic frequency multiplier will be developed for each desired output frequency. The generators could be an integral part of the bandpass filter. The harmonic generator will be released for mechanical packaging during the next quarter.

c. Mixer Input Bandpass Filter

Initial consideration was given to the use of electronically tunable bandpass filters, i.e., yttrium-iron-garnet spheres. While YIG program control circuitry is feasible, this approach was not considered practical due to the temperature sensitivity of these units.

An alternate method is to provide a fixed filter at each of the ten harmonics. Specifications for the input filters were outlined and called for 10 Mc bandwidths centered at each of the 7th through 16th harmonics (of the 100-Mc signal) supplied by the Harmonic Generator. These bandpass filters are being designed for 70 db rejection at $f_o \pm 50$ Mc.

During the next quarter, the design of these filters and breadboard tests will be completed; the filters will be released to manufacturing.

d. Mixer

The up-converting crystal mixer was designed in coax. It is here that the 300-Mc to 400-Mc signal from the Frequency Synthesizer is mixed

with any one of the ten frequencies from the harmonic generator. The intermediate frequency input must be designed to pass the 300-Mc to 400 Mc signal while rejecting the harmonic signals from 700 Mc to 1600 Mc injected at the local oscillator part of the mixer. Some tests have been performed to evaluate the generation of harmonics of the IF signal which fall in the output frequency band. It has become evident that high level mixing can not be tolerated but that external bias on the mixer will be needed to optimize the ratio of the desired sum frequency signal level to spurious undesired signal level in the output. With mixing done at low levels it is imperative that losses be minimized throughout the circuit so that adequate driving power is maintained at the TWT amplifier.

During the next quarter the mixer will be breadboarded, combined with the associated bandpass filters, and tested.

e. Mixer Output Bandpass Filter

The output filters are required to reject unwanted carrier and sideband signals which are a minimum of ± 300 Mc from the center frequency. The filters were designed to provide 30 db rejection at ± 250 Mc and to provide a pass band of 100 Mc. Calculations showed that four resonant sections were needed in each filter to meet specifications. Calculations were based on the low pass prototype and general formulas were used to obtain element values that yield the Tchebycheff insertion loss response. Graphs and nomographs by Cohn were used to obtain the printed guide strip dimensions and spacings.

Three experimental designs of the output filters at the high, middle, and low ends of the band were constructed and tested to verify the dimensional calculations. The overall shape of the response was good, but the center frequency was too low by one-fourth the bandwidth.

A new set of dimensions has been calculated and a new set of sample filters is being etched. During the next quarter tests have been conducted on the diode switches which are in series with the bandpass filters. A printed circuit test jig was built and serveral types of computer type diodes were evaluated. Maximum attenuation across the diode was obtained with a slight reversal of bias; measured values ranged from 10 db to 17 db. Since a minimum total inband rejection of 40 db through the diodes is desired, four diodes in series will be used. Minimum insertion loss for the diode switches ranged from 0.4 to 1.5 db per unit.

During the next quarter, design and breadboard tests will be completed; the filter will be released to manufacturing.

f. TWT Amplifier

Supplier proposals on traveling wave tubes were received and are under evaluation. An order for the TWT will be placed during the next quarter, upon completion of evaluation. When the tube is received its performance will be evaluated.

g. TWT Filament Power Supply

Design will begin as soon as the TWT is selected.

h. Coaxial Switch

The SPDT coaxial switch, a standard item, will be ordered during the next quarter.

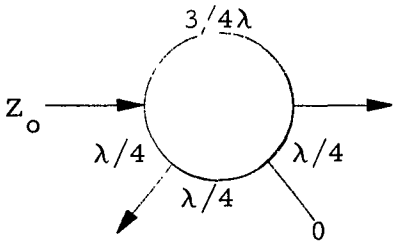
C. L-Band Conversion Circuits

a. Single-Sideband Modulator

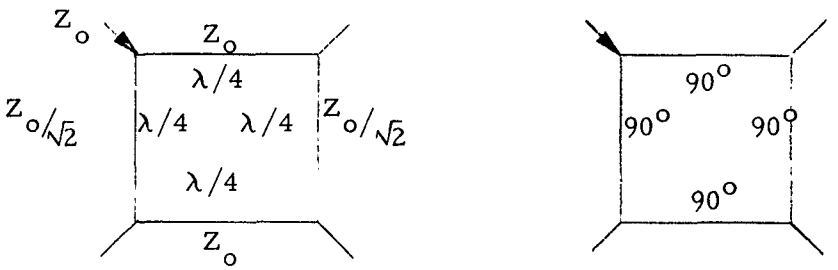
A block diagram of the L-Band Conversion Circuits is shown in Figure 6-4.

The single-side band modulator is being designed from 3 TEM line broadband magic tees and one TEM line broadband quadrature hybrid. Because the YIG filter will not be used, it is necessary to develop a modulator which has 20 db carrier and sideband suppression.

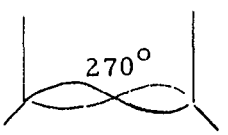
Of the two types of coaxial hybrids, the quadrature type is available, but the Magic T type is still under design. The usual configuration is



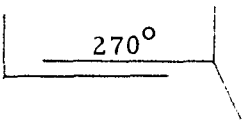
When converted to stripline this becomes



But, the MTE SSB Modulator requires that the bottom leg be 270° long. One supplier is attempting to obtain this by inserting a half-turn twist in the two strips



This adds a 180° difference to the 90° length, giving a total of 270°. Another approach being taken to obtain the additional 180° involves separating the two strips by the proper amount:



Models of these hybrids are being constructed; it is expected that evaluation will be completed by the end of the next quarter.

b. Ratiometer

The ratiometer performs two functions: (1) It measures VSWR of equipment placed at the output connector; and (2) measures attenuation of a transmission line placed at the output connector. Associated with the ratiometer is a termination having a VSWR of 1.5; this termination can be switched in to check ratiometer operation.

The L-Band Ratiometer is built on the same general principles as the X-Band Ratiometer described in paragraph 6.1.2 J. The major difference between the design of the two systems is in a part of the variable attenuator. At L-Band there are larger error-producing factors in the mismatch of the switches, in the insertion losses of the switches, and in the attenuation errors of the attenuators. For these reasons the L-Band variable attenuator will be a composite of one switch and attenuator, and one diode attenuator similar to that used in the RF Leveler.

The diode attenuator consists of a coaxially-mounted diode, a 10 db sampling coupler and thermistor detector, and a comparator circuit feeding back to the attenuator diode. Because of the power levels

necessary for the thermistor, the diode attenuator is mounted in the main line between the incident wave sampling coupler and the reflected wave sampling coupler. This arrangement makes it necessary to use two directional couplers rather than a bedirectional coupler. Because the diode attenuator is reflective, it is necessary to place isolators on both sides of the diode.

Parts for the ratiometer have been ordered. Breadboard construction and test will be completed during the next quarter.

c. Variable Attenuator

The 20 db variable attenuator was ordered, but because of the possibility that it may not meet specifications for attenuation accuracy, construction was started on directional couplers which can be adjusted to vary attenuation. During the next quarter, the purchased variable attenuator will be tested, the adjustable directional coupler will be evaluated, and a decision will be reached on the type of attenuator to be used.

d. Leveler

The L-Band Leveler uses the same circuit as the leveler in the X-Band Conversion circuits described in paragraph 6.1.2.4 but the microwave components are different. Breadboard construction began during this quarter; construction and testing will be completed during the next quarter.

D. L-Band Input and Output Circuits

A simplified block diagram of the L-Band Input and Output Circuits is shown in Figure 6-5. The 50-db attenuator consists of three transfer switches which insert or remove three fixed attenuators (10, 20, and 20 db).

The power monitor is a temperature compensated thermistor type. A crystal detector is included to provide for pulse measurements. Several crystal detectors were evaluated, but were found to be out of specification requirements, particularly at the low end of the band. This defect was attributed to the method of providing the dc return in the mount. Mounts of different construction have been obtained and will be evaluated during the next quarter.

The leveler contains a reactive diode and is capable of programming attenuation from 1 to 10 db in 1 db steps.

The 100 db attenuator consists of four networks which insert or remove four fixed attenuators (10, 20, 40 and 40 db). Transfer switches can be used for the 10 db and 20 db sections, but the 40-db attenuators employ single pole switches at each end of the attenuator. Crosstalk of coax switches is only about 40 db; by using a switch at each end, the crosstalk around the 40-db attenuator is increased to 80 db.

During the next quarter breadboards of the power monitor, leveler, and attenuators will be constructed; testing will be completed.

E. L-Band Coupler and Dummy Load

The components of this package are designed to handle 1 kw average power and 50 kw peak power. The main transmission line will be 1 5/8-inch coaxial line, and the coupled line will have an output to

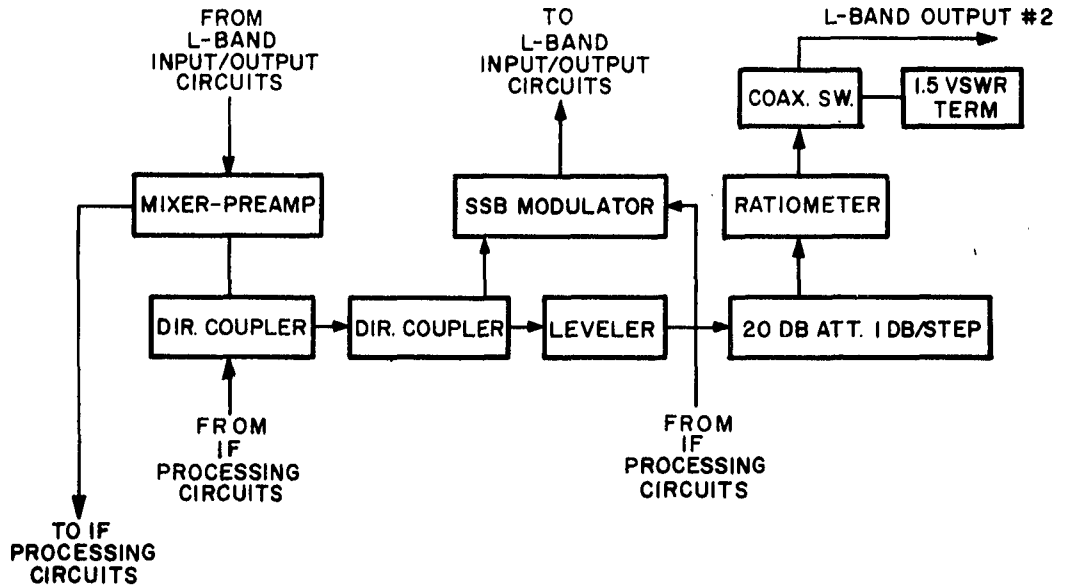


Figure 6-4. L-band conversion circuits - block diagram

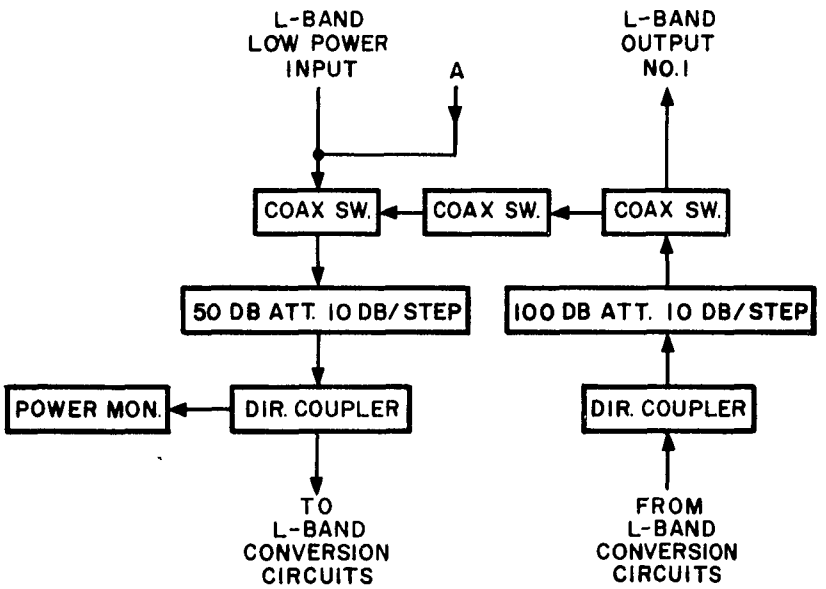


Figure 6-5. L-band input/output circuits-block diagram

type N coaxial line. The line size was chosen to allow versatility in the units to be tested since short transitions from 1 5/8 inch line to most other sizes are readily available.

It is planned to use a convection-cooled load to simplify circuitry. If the forced-air cooling becomes necessary, a temperature measuring warning circuits will be provided to signal when the load becomes overheated.

This package is being released for quotations.

Delivery is expected in the second quarter of 1963.

F. Microwave Synthesizer

A block diagram of the Microwave Synthesizer is shown in Figure 6-6. The microwave synthesizer is a new chassis; it uses components taken from the L-Band and X-Band Extender circuits when they were redesigned. The synthesizer takes the swept output (1-2 Gc)of the L-Band extender and mixes it with selected harmonics (1 Gc and 2 Gc) of the L-Band extender output (25 Mc). Output will be 1-4 Gc in three steps (1-2 Gc, 2-3 Gc, and 3-4 Gc).

A potential problem area in the Microwave Synthesizer chassis is expected in the two mixers, one mixing 1 Gc with 1-2 Gc, and the other mixing 2 Gc with 1-2 Gc, because the input signals and output signal are close in frequency. These problems should be solved by using filters- low pass on the input lines and bandpass on the output lines. An associated problem on the 1 Gc plus 1-2 Gc mixer occurs when 1 Gc is mixed with 2 Gc to obtain 3 Gc. The output of this mixer must be capable of passing 2-3 Gc; therefore when 1 Gc and 2 Gc are mixed to generate 3 Gc, there are two frequencies present (2Gc and

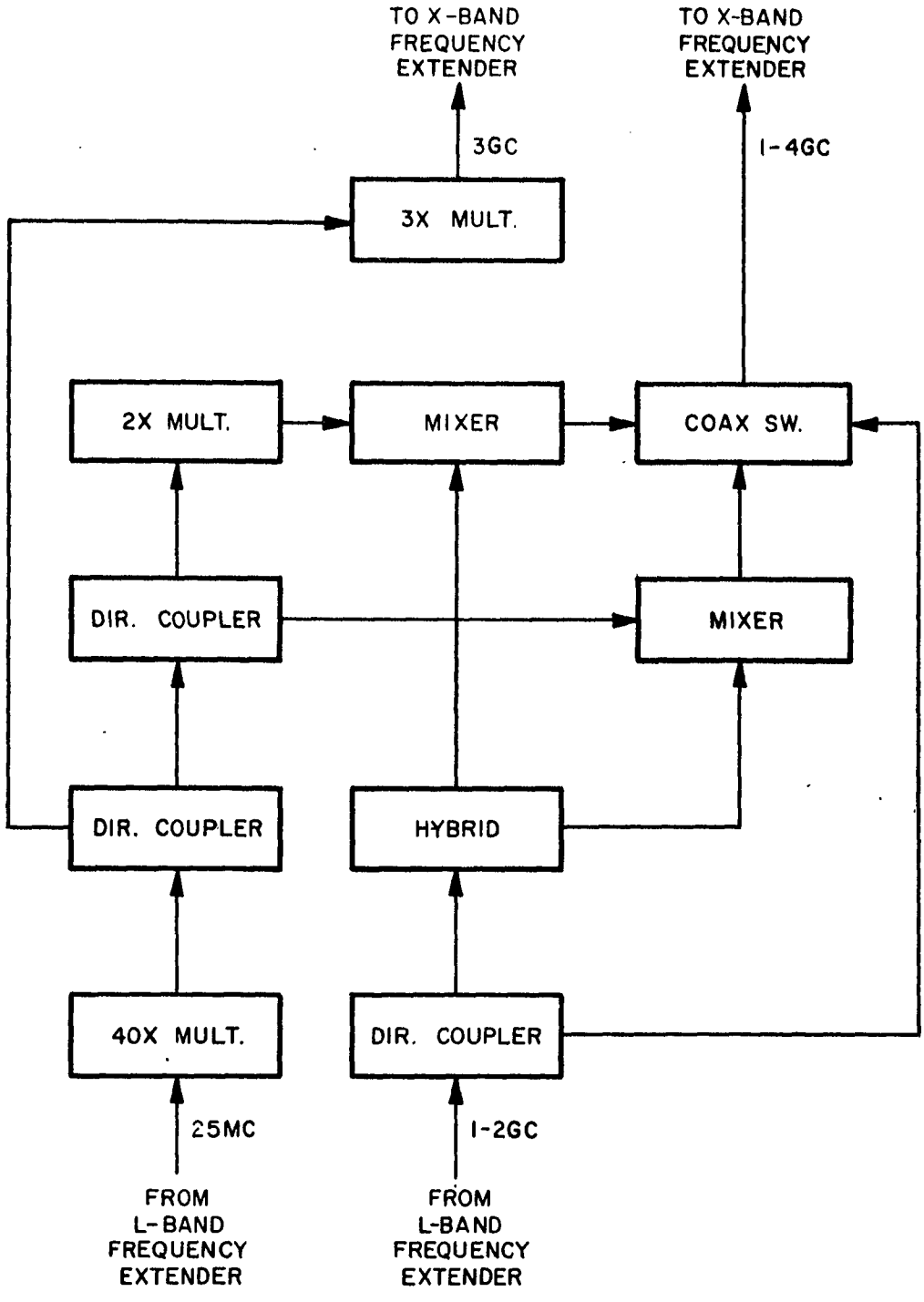


Figure 6-6. Microwave synthesizer - block diagram

3 Gc) which may be passed by the output bandpass filter. To avoid this, the 1-2 Gc input must be isolated from the 2-3 Gc output. The approach being used to solve this problem is to use single sideband modulator techniques for carrier suppression.

During the next quarter preliminary design of the mixers with their associated filters and combining circuits will be completed. A breadboard will be constructed, and testing effort will be concentrated on evaluation of the high power mixing process.

The directional couplers, as standard items, were defined and ordered.

The hybrid, a standard TEM mode coaxial unit, was received and satisfactorily tested.

Specifications for the X2 and X3 multipliers were developed. These long lead items were ordered; delivery is expected near the end of the coming quarter. The multipliers will be tested at MTE power levels.

Preliminary circuit design for the X40 multiplier was completed; and components have been ordered. During the next quarter breadboard testing will be completed.

G. X-Band Frequency Extender

A diagram of the X-Band Frequency Extender is shown in Figure 6-7. The X-Band Frequency Extender design has been superseded by a more reliable and efficient system. The Frequency Extender formerly consisted of a single harmonic generator (responsible for the generation of 7, 8, 9 and 10 Gc) and a single mixer producing the summation of the harmonic generator signals and the 1 to 2 Gc L-Band Frequency Extender signal.

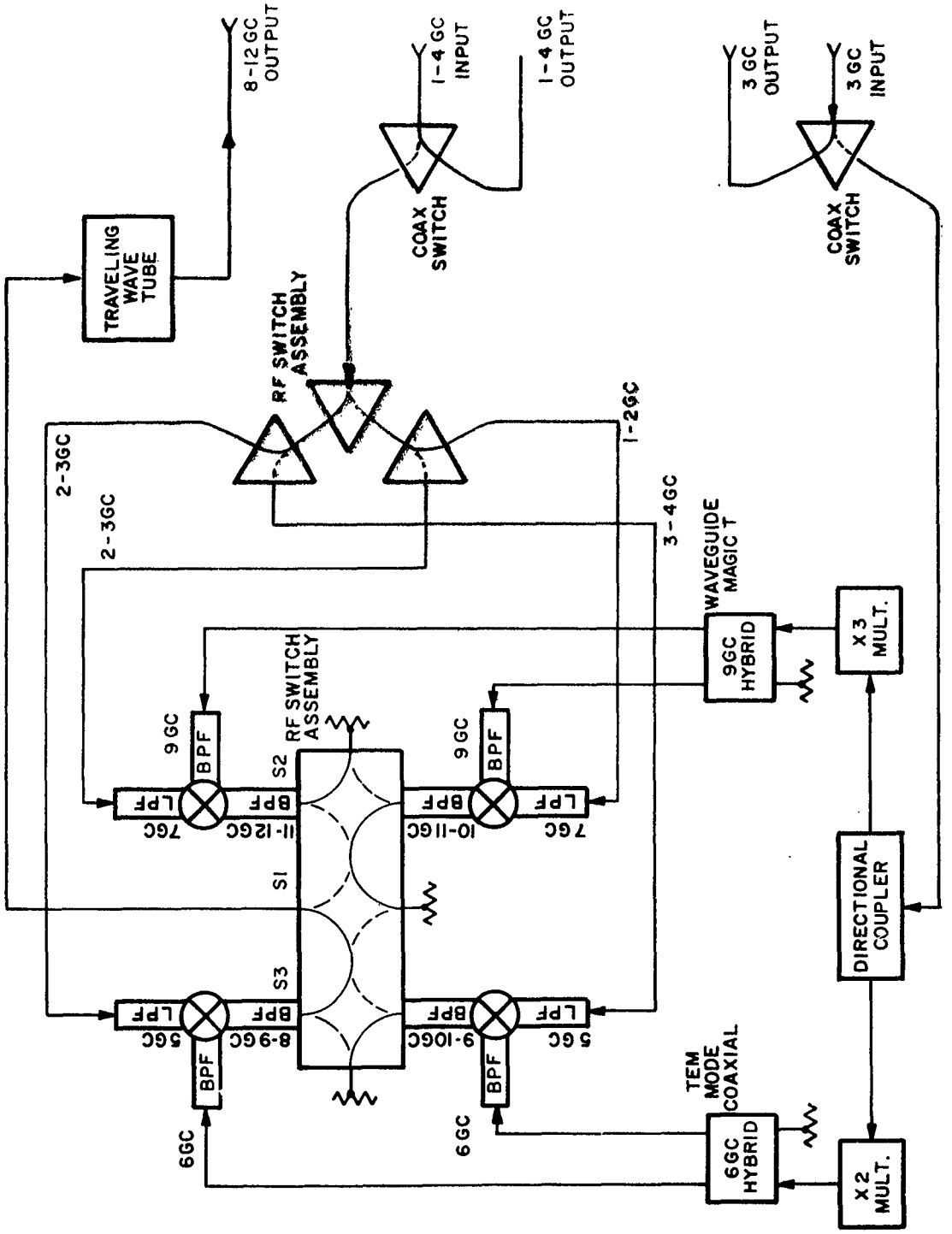


Figure 6-7. X-band frequency extender - block diagram

As shown in Figure 6-7, a 3-Gc signal from the Microwave Snythesizer is fed to a directional coupler whose outputs are applied to a doubler and a tripler. The 6-Gc and 9-Gc outputs of the harmonic generators are divided in hybrids and fed as local oscillator inputs to the mixers. A stepped signal from the Microwave Synthesizer in the range of 1 to 2, 2 to 3, or 3 to 4 Gc is fed through programmed coaxial switches into the mixer signal inputs. The upper sideband generated by the action of the mixer is sent through specially-designed filters to a bank of programmed waveguide switches where each signal is, in turn, connected to the traveling wave tube input.

The X-Bank Frequency Extender mixers are designed to accept the signal inputs via a coaxial low pass filter and the local oscillator power via a narrow bandpass filter. The low pass-bandpass filter combination provides reasonable local oscillator to signal isolation.

A prototype mixer is being fabricated and will be available for laboratory testing. The testing of the mixer will be aimed at achieving efficient operation with low spurious signal levels.

A power monitor will be incorporated in the X-Band Frequency Extender as an indicator of unit operational capability. The power monitor (which will sample the traveling wave tube amplifier output) will consist of a directional coupler and a Microwave Associates MA462 monitor diode. Failure of the unit to attain sufficient output power will be indicated by a panel mounted light.

Traveling wave tube protective means, metering and filament circuitry will be located in the X-Band Frequency Extender assembly to minimize the number of high voltage leads to the Dual Traveling Wave Tube Power Supply.

A preliminary design of the TWT filament supply has been accomplished. It consists of a high voltage isolation transformer followed by a full-wave rectifier and a two transistor series regulator circuit.

The transformer used to develop the filament voltage also has a winding for generation of a zero to -50 volts TWT grid bias. Bias voltage is developed by means of a half-wave rectifier bollowed by a zener diode shunt regulator.

Helix current is monitored by means of a resistor placed in series with the ground return. An indication of excessive helix current results in the removal of the TWT high voltage.

During the next quarter, this filament supply will be breadboarded and the circuit finalized.

The hybrids were evaluated with satisfactory results.

The X2 and X3 multipliers are on order. Since they are the same as those used in the Microwave Synthesizer, delivery is expected near the end of the next quarter.

Directional couplers, waveguide switches, and the TWT were ordered. The TWT will be checked out first with laboratory power supplies and, toward the end of the next quarter, will be tested with the MTE power supplies.

A complete breadboard will not be constructed, since checks on the individual components will be sufficient in most cases. Design of this unit will be completed during the next quarter.

H. X-Band Conversion Circuits

A block diagram of the X-Band Conversion Circuits is shown in Figure 6-8. A significant change has been incorporated in the conversion circuits: the electronically tuned filters (YIG filters) are no longer required because the SSB modulators have demonstrated sufficiently high sideband rejection.

a. Mixer-Preamplifier

The single ended 1N1132 mixer obtains local oscillator signals from the X-Band Input and Output Circuits assembly through a 10 db coupler (not shown in Figure 6-8) housed within the Mixer-Preamplifier unit. Bias for the mixer diode is obtained from the X-Band Frequency Extender through a 10-db directional coupler, which feeds the 10 db coupler in the Mixer-Preamplifier. Several different crystal mounts are being evaluated for optimum performance across the band; results will be available during the next quarter.

The preamplifier, a 3 stage video amplifier with 20 db gain, will be breadboarded and tested during the next quarter.

b. Leveler and Attenuator

The leveler will produce 10-db attenuation in 1-db steps and the attenuators will be adjustable in 10-db steps. With this combination 120 db of attenuation is obtainable in 1 db steps.

A description of the leveler, precision attenuators and associated switches is similar to that for the X-Band Input and Output Circuits (See paragraph I.). no breadboarding or testing is contemplated because results of the X-Band Input and Output Circuits tests will apply here.

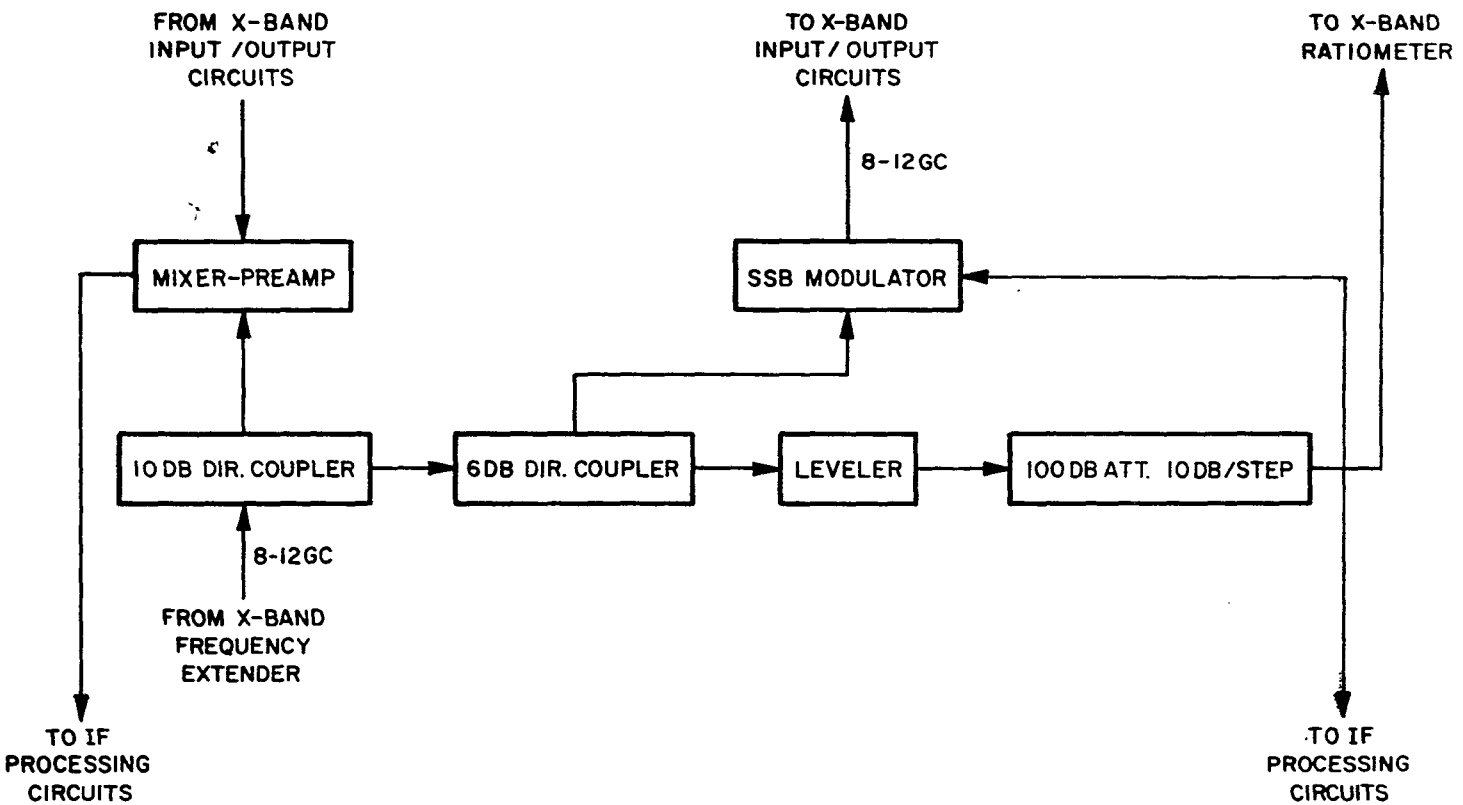


Figure 6-8. X-band conversion circuits-block diagram

c. Single-Sideband Generator

From the through arm of the 6 db directional coupler the microwave energy is controlled in power level to the balanced modulator SSB Generator by a ferrite variable attenuator. Control for the attenuator which operates on the Faraday Rotation principle is supplied by the RF leveler.

The SSB Generator translates the input microwave signal by the modulating frequency. For the X-Band case, this will be either 10 or 30 Mc supplied in quadrature through 3 programmed coaxial switches to the balanced modulators.

The original concept for accomplishing single sideband generation was by the use of a bucking rotator ferrite phase shifter for the microwave quadrature signal. Tests of the phase shifter indicate an approximately linear relationship between coil current and phase shift over 25% of the band. Further attempts to increase its broadband coverage have been suspended because the use of the programmed phase shifter is considered too complex for this system; similar results are expected with the completely broadband SSB Generator described below (see Figure 6-9).

The broadband SSB Generator utilizes 3 matched magic tees, 4 matched detector mounts, 2 pairs of matched tripolar crystals and a special 3-db directional coupler.

An incoming microwave signal is split equally in amplitude and phase by the input magic tee and applied to the balanced modulators. Each balanced modulator produces a double sideband suppressed carrier output. The output sidebands are combined in the 3 db directional coupler in a manner such that the upper sideband is propagated out of the through arm while the lower sideband is terminated in a waveguide

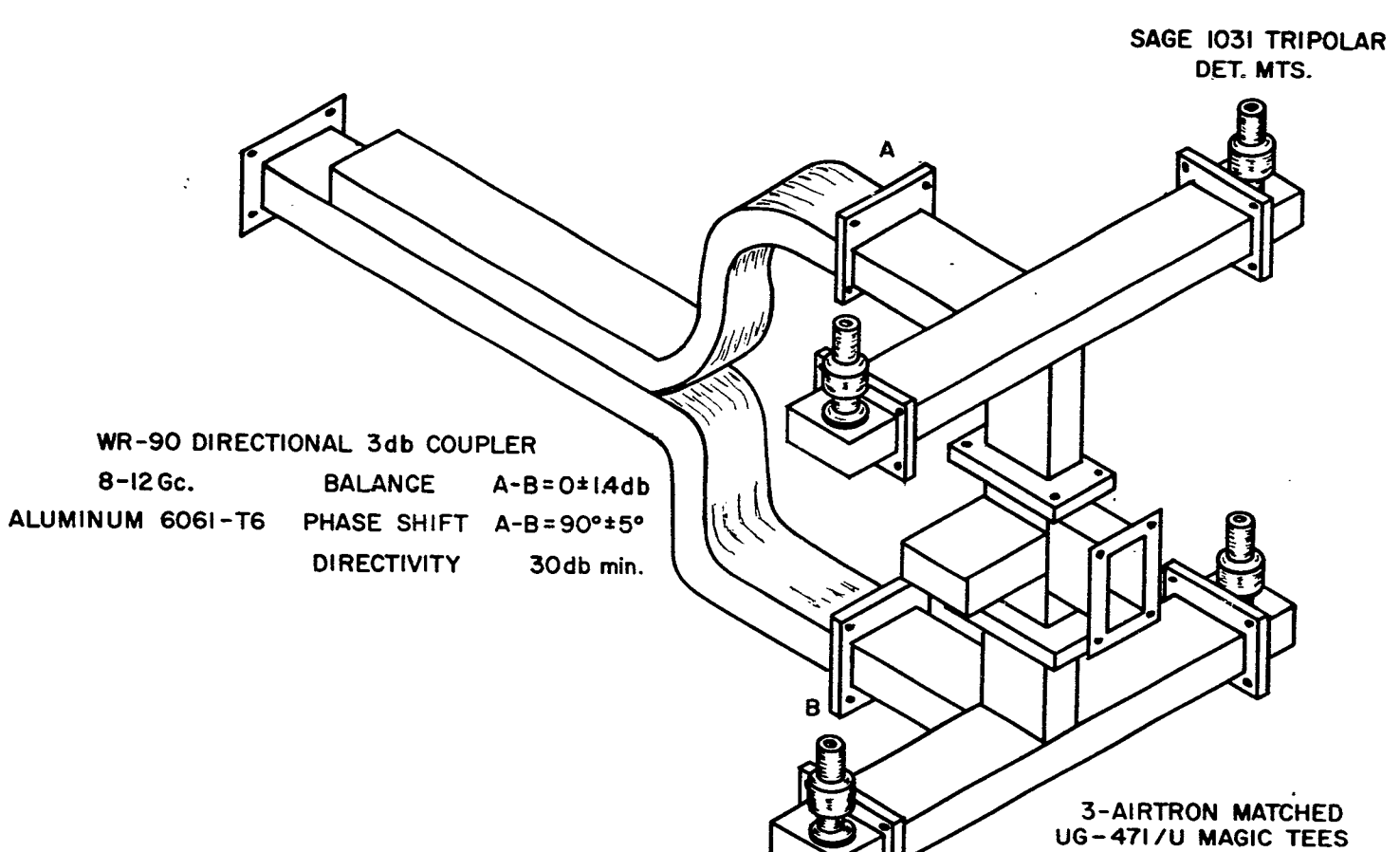


Figure 6-9. X-band single sideband generator

load in the coupled arm. A convenient means of monitoring the microwave output of the SSB Generator is to replace the load with a detector mount and threshold indicator. The detected signal is the counterpart of the output signal.

Tests of one of the balanced modulators indicate approximately 25 db suppression of carrier and unwanted higher order sidebands compared to the desired sidebands for 25% of the band. Over this frequency range the input microwave power was allowed to deviate 3 db with a corresponding change in sideband output level of 1 db. This indicates the SSB Generator is itself an RF Leveler. During one of these tests with the microwave input power held constant, the conversion loss improved approximately 1 db over the lGc range (8.5 to 9.5 Gc). An explanation for this deviation would be that the vswr of the detector mounts and crystals was changing with frequency. A vswr measurement of the individual detector mounts with the same crystal installed verified this assumption. Mechanical inspection and measurement of one holder showed it's crystal shoulder and height positioning of the center pin differed from the other three, creating a discontinuity at the junction, therefore causing an increase in the vswr indication.

The above tests were made with double sideband components. During the next quarter the single sideband generator will be breadboarded and tests will be completed.

d. Leveler

Use of dual peak detectors has proven successful for regulating microwave power.

Circuit design has progressed, but further design is required in three areas - preamplifier drift, preamplifier gain, and crystal detector

flatness. Figure 6-10 shows the leveler in block diagram form. Analysis of this loop is underway: a breadboard assembly will be constructed to develop a practical circuit which meets drift and gain requirements when using available crystals. The deviation of the crystal detectors from constant sensitivity across the required band continues to be excessive. The original solution to this problem was to introduce correction signals for several regions of the total spectral band to be covered. This method requires many control circuits and has been replaced by development of a broadband crystal monitor. Moderately broadband waveguide to coax transitions will be used in combination with dc return crystal mounts and tripolar crystals. The impedance at the circuit terminals of the crystal will be increased and the effect of its variation will be determined.

I. X-Band Input and Output Circuits

This unit (see Figure 6-11) combines the functions of those units previously described as X-Band Input Circuits MTE 5842 and X-Band Output Circuits MTE-5843.

Breadboards of the attenuator assemblies were completed. A combination of waveguide transfer switches and precise fixed rotary vane attenuators is programmed by a BCD signal. Performance evaluation of the attenuators and switches will be made during the next quarter.

Circuits for the RF Leveler and Power Monitor were developed. The original concept for the monitor was to read average values because of MAULER characteristics, but this has been changed to peak reading to accommodate the general case. Breadboards of these units will be constructed during the next quarter; major effort required will be in optimizing the broadband performance of the detectors.

It is expected that the X-Band Input and Output Assembly will be released to drafting during the next quarter.

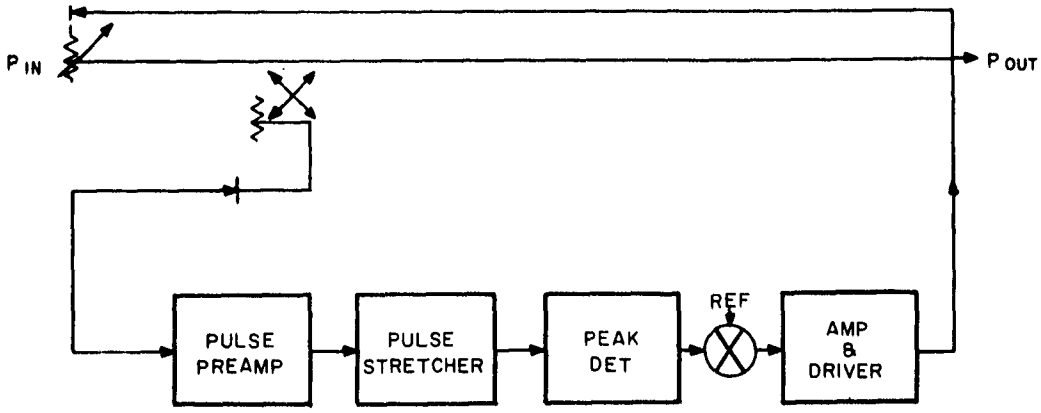


Figure 6-10. X-band RF leveler

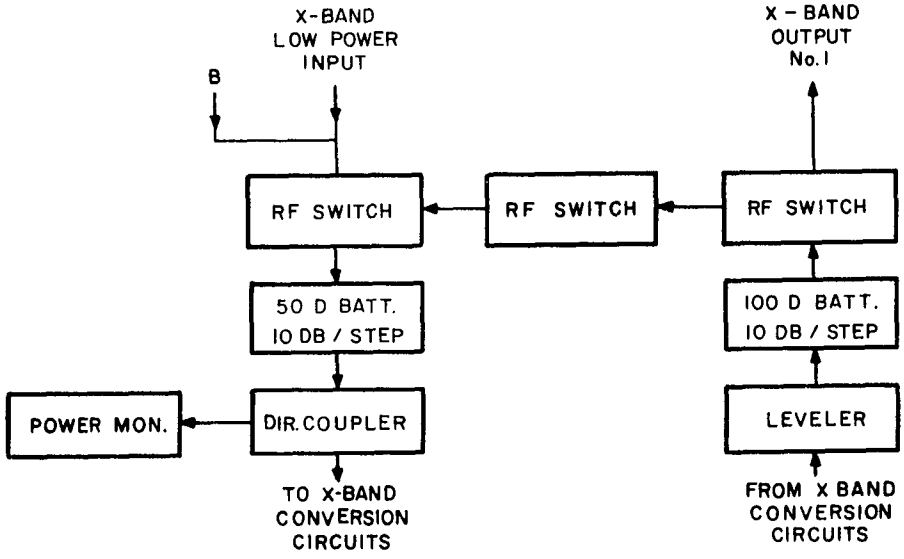


Figure 6-11. X-band input/output circuits - block diagram

J. X-Band Ratiometer Assembly

The ratiometer performs two functions: (1) It measures VSWR of equipment placed at the output connector; and (2) measures attenuation of a transmission line placed at the output connector. Associated with the ratiometer is a termination having a VSWR of 1.5; this termination can be switched in to check ratiometer operation.

Two changes were made in the basic approach used in the Ratiometer Assembly. The first alteration was the location change of the variable attenuator. The original approach was to attenuate the incident sampled wave down to the level of the reflected sampled wave and, by knowing the amount of attenuation necessary, to automatically compute the reflection coefficient. This approach required a fairly large dynamic range ($\sim$ 30 db) over which both crystals had to remain matched.

The new approach (see Figure 6-12) places a fixed attenuator in the incident wave sampling arm to attenuate the power to the lowest level at which it is desired to perform detection in the reflected wave sampling arm. The variable attenuator is placed in the reflected wave sampling arm to attenuate the power down to the level of the power in the incident wave sampling arm. The reflected wave sampling arm now measures only the power reflected from a mismatch. With these power levels into the ratiometer the dynamic range of the crystals will be near zero

The second change is in the design of the comparator and attenuation control circuits. In the new design is (1) the computer will drive the variable attenuator and (2) a null signal to the computer will stop the attenuator from searching. At the time of a stop search, the computer will read out the value of attenuation and convert this to a reflection coefficient.

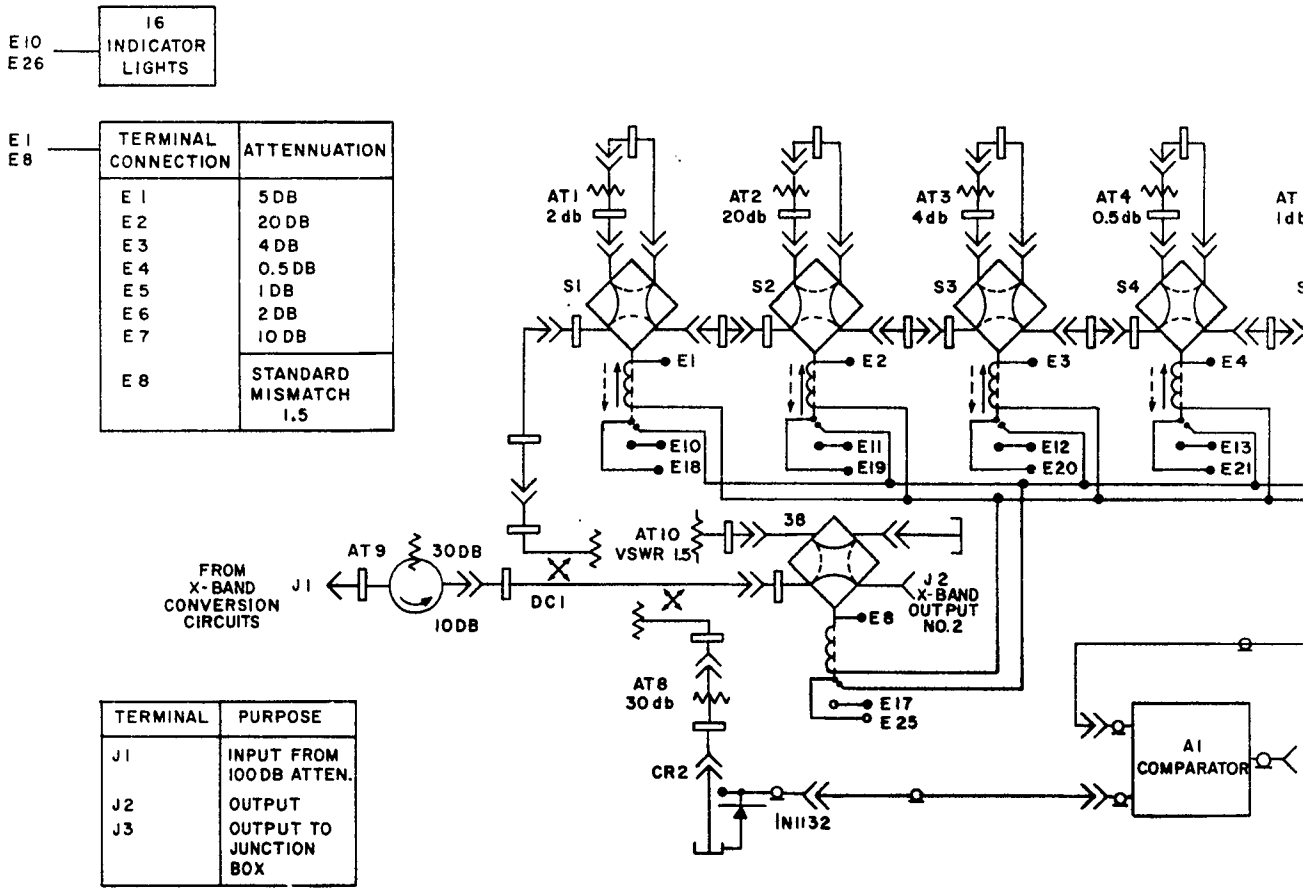


Figure 6-12. X-band ratiometer - block diagram

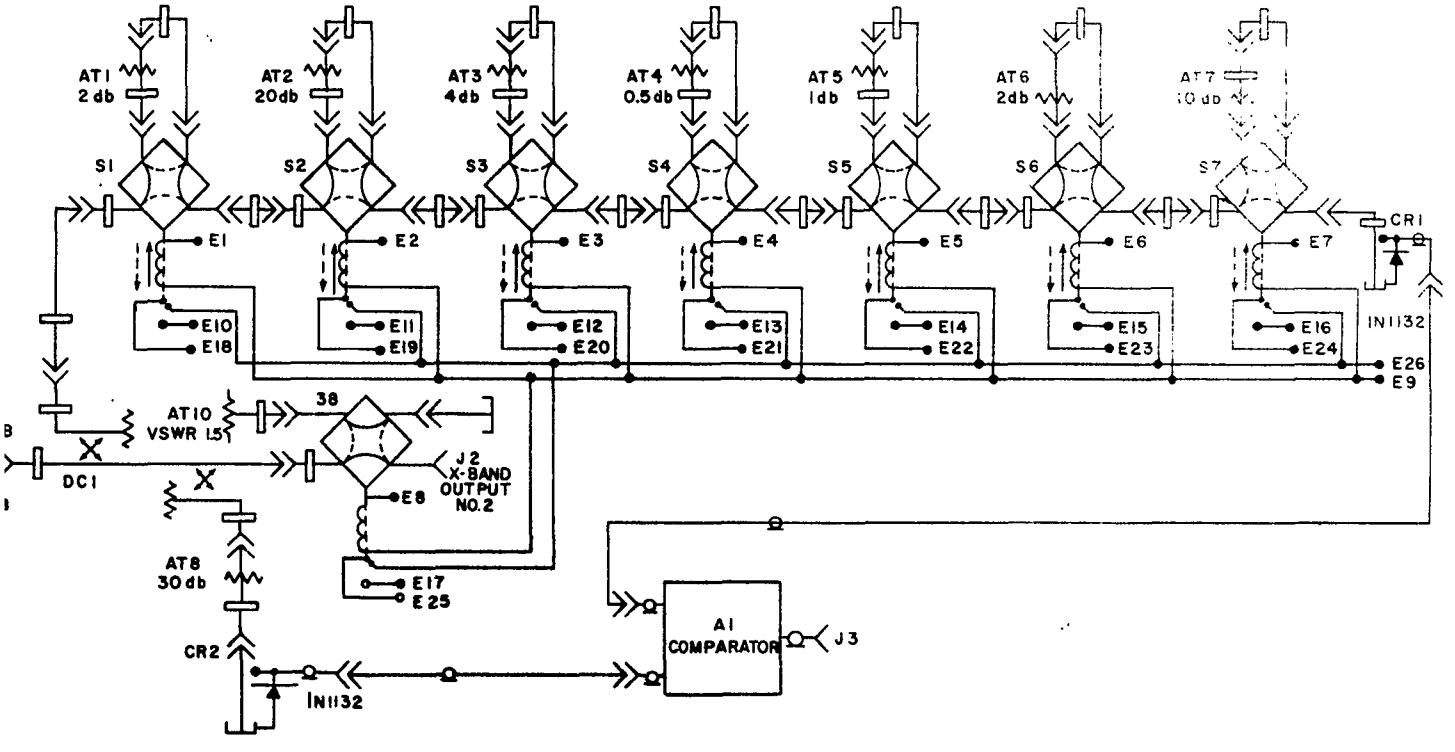


Figure 6-12. X-band ratiometer - block diagram

With the limited time available for development, the best variable attenuator design is that using waveguide transfer switches and fixed rotary vane attenuators; this provides the ability to switch various fixed values of attenuation in or out. The units are arranged in series so that their values are additive. Since the computer sets the attenuators in or out of the line, readout is a simple matter.

One addition has been made to the original plans for the ratiometer. This is a self-check capability employing a transfer switch and a standard mismatch. These components are placed at the output of the ratiometer with the transfer switch switching the main line either to the standard mismatch or to the test piece connecting flange.

Parts for a breadboard model are either on order or soon to be ordered.

During the next quarter, directional couplers will be tested for VSWR, coupling, and directivity across the band. Crystal detectors will be checked for VSWR and voltage output with constant power input. The attenuator assembly will be tested for attenuation and VSWR. The standard mismatch will be evaluated across the band. A breadboard of the complete assembly will be constructed and tested.

K. X-Band Coupler and Dummy Load

The components of this package are designed to handle 2.5 kw average power and 250 kw peak power. It is planned that the load will be convection cooled. If forced air cooling becomes necessary, a temperature measuring warning system will be provided to indicate overheating of the load.

The package is now out for quotation, and a final decision with respect to cooling should be reached by the end of January 1963.

L. IF Processing Circuits

The IF processing Circuits in simplified block diagram form are shown in Figure 6-13.

a. Frequency Search Circuit

The frequency search circuit was designed and tested. The design consists of an FM discriminator driving a low pass filter for cw signals and a pulse integrator for pulsed signals. These outputs drive an OR gate which actuates a Schmidt trigger to produce the stop search signal.

A narrowband filter was considered for this function instead of the discriminator, but this did not appear to provide the desired degree of accuracy. The triggering circuits (low pass filter, pulse integrator) and Schmidt trigger are arranged to provide the stop search signals after the IF frequency is such that the discriminator output (dc or pulses) is negative for 150 to 200 seconds. This eliminates the possibility of short transient signals in the IF causing a stop search signal to be produced. This technique requires that the synthesizer remain on one frequency longer than 200/duty cycle microseconds.

b. Pulse Modulator

The pulse modulator, as designed, produces 35 db on-to-off ratio. The microwave SSB modulators require at least 40 db; therefore, it is planned to use two modulators in series to produce over 50 db on-to-off ratio. The pulse modulators have sufficient bandwidth to accommodate the 9.4 Mc, 10.4 Mc, and 30 Mc signals with one input.

c. Discriminator

The circuitry to measure FM deviation consists of the stop search discriminator driving a constant gain amplifier followed by a peak-to-peak

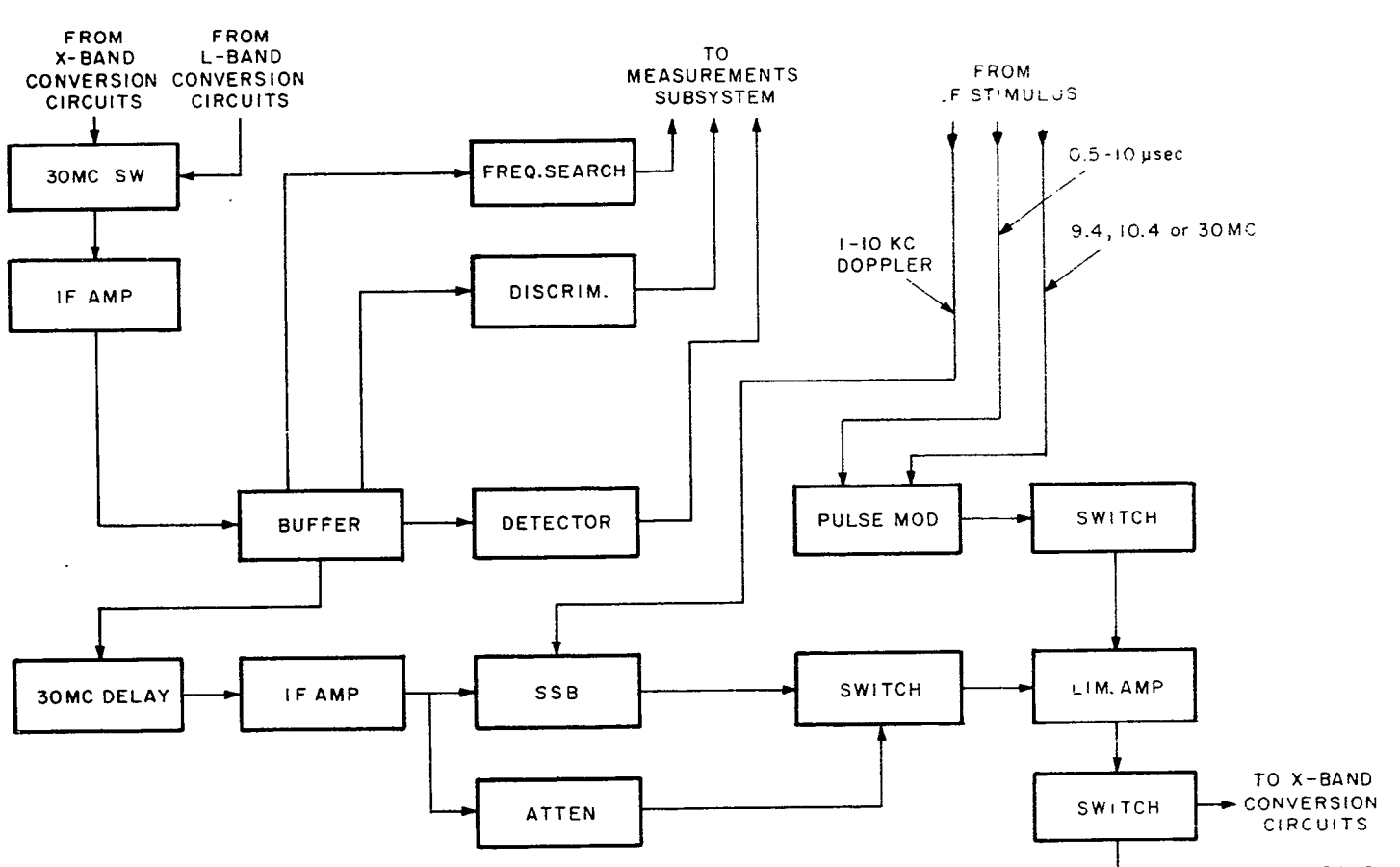


Figure 6-13. IF processing circuits - block diagram

detector which produces a voltage indicating total deviation. This system appears adequate, however, adjustment is critical. Another system which will be self-calibrating is being designed and tested. This alternate system calls for sending a signal with known deviations into the discriminator and generating the UUT deviation signal based on comparison with the known deviation.

d. Limiter Amplifier

A wideband amplifier has been designed which produces a constant output over a wide range of input signals.

e. 30-Mc Single-Sideband Generator

The single-sideband generator uses the phasing technique for sideband separation. Filters can not separate the sidebands. A 30-Mc LC octave wide quadrature hybrid has been purchased and tested. It did not meet specifications for equality of output and was replaced by the manufacturer. An RC audio (Doppler input) quadrature network is being designed with a decade bandwidth.

f. 30-Mc Delay Line

Requests for quotes have been sent out for a 30-Mc quartz delay line with 15 Mc bandwidth. This bandwidth will allow preservation of rise times as short as 0.05 μsec. One percent delay tolerance and a moderate temperature range of operation will allow the use of an unheated line. The insertion loss of the delay line will be on the order of 50 db; hence an IF amplifier follows it.

g. 30-Mc IF Amplifier

The 30-Mc IF amplifier is essentially a 90-Mc video amplifier with a bandpass filter approximately 15-Mc wide. The use of a wideband video

amplifier will allow adaptability to a 60-Mc IF which is required for future systems with bandwidths greater than 15 mc. Design work has been started using cascaded collector to base feedback, common emitter connected 2N918 transistors.

h. Plans for the Next Quarter

Evaluation of the breadboards and electrical design will be completed; final packaging will begin.

M. Dual Traveling Wave Tube Power Supply

Initial design has begun. Final choice of traveling wave tubes has not been made; therefore it was necessary to choose a power supply design which would provide maximum flexibility as far as output voltage and current are concerned. The design is completely solid-state except for a corona voltage-regulating diode.

The major design goals are tabulated below:

	Supply No. 1	Supply No. 2
Output voltage	750-1200 Volts	2000-2500 Volts
Output current	40-80 ma	20-35 ma
Load regulation	1% maximum	1% maximum
Ripple	0.001% maximum	0.001% maximum
Short-circuit protection	yes	yes
Efficiency	75% minimum	75% minimum

Figure 6-14 shows the type of regulating circuit used in the supply. A dc controlled asymmetrical multivibrator generates rectangular pulses at a constant pulse-repetition frequency. The pulse width being a function of the voltage difference between a dc reference and the

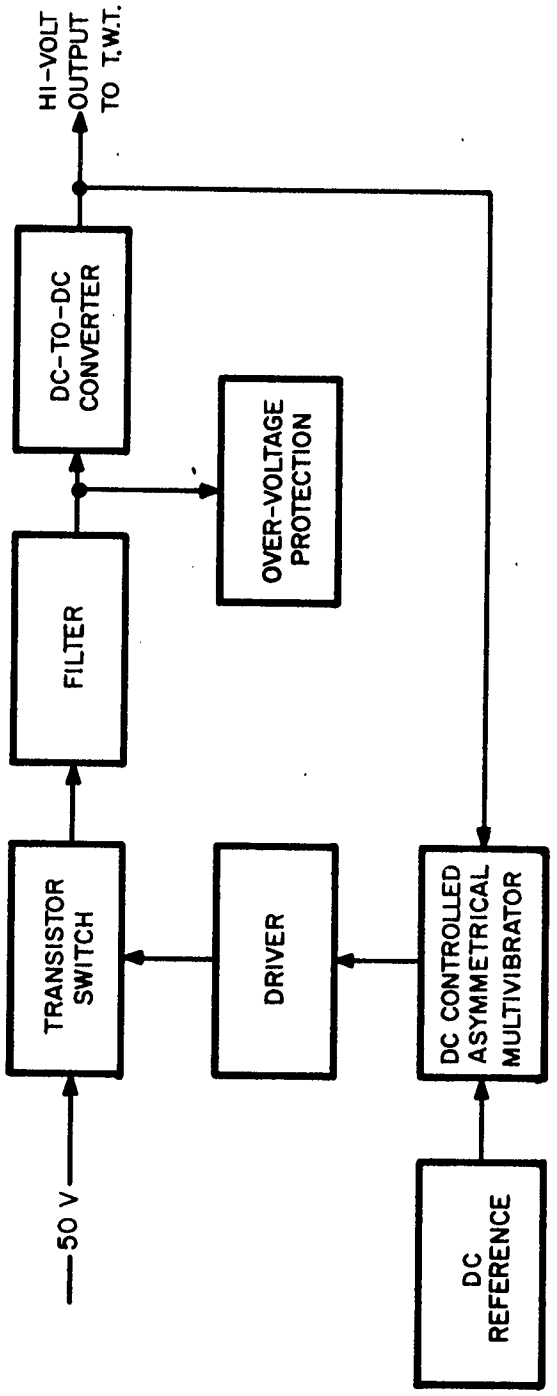


Figure 6-14. TWT regulating circuit - block diagram

output of the dc-to-dc converter. When the converter output voltage is lower than desired, the multivibrator output pulses widen. The output of the asymmetrical multivibrator is impressed on a driver stage which gates a transistor switch on for the duration of the multivibrator output pulse. The dc-to-dc converter is a Conventional free-running multivibrator circuit. Feedback to the asymmetrical multivibrator is provided by means of a pick-off at the junction of a high-voltage corona regulating diode in series with dropping resistors. Thus, changes in output voltage are sensed and a change in the dc-to-dc converter input voltage is effected to correct the error.

An over-voltage protection circuit monitors the dc voltage being fed to the dc-to-dc converter. This voltage is related to the power supply output voltage by a known constant. Thus, if a voltage into the dc-to-dc converter is sensed which might result in damage to the traveling wave tube, a relay is activated to remove the -50 volt input from the transistor switch.

The pulse-repetition frequency of the asymmetrical multivibrator is expected to be chosen in the range of 2 to 5 kc, and the frequency of the dc-to-dc converter is expected to be 400 cps.
The reasons which led to the choice of this circuit are:

(1) Flexibility - Large output-voltage changes can be effected by modifying the turns ratio of the dc-to-dc converter step-up transformer and by selecting a new corona regulator.

(2) Solide-state considerations - For reliability reasons it is desirable to use a completely solid-state design. The alternate approach of using a series regulator would require several hundred volt drop in the regulating element;this is not feasible with present solid-state devices.

(3) Efficiency - Greater efficiency is achieved because there is no surplus power to be dissipated in a switching type regulator.

(4) Short-circuit protection - The dc-to-dc converter portion of the proposed regulator provides built-in short-circuit protection. A short-circuit across the output of this supply causes the free-running multivibrator to cease operation, thus stopping generation of high voltage.

The breadbord of this unit will be assembled and tested during the next quarter.

N. Junction Box

The functions that this unit must perform are being determined. As a minimum it must distribute the digital input signals from the computed controller to the appropriate location as well as decoding and logic for setting up the frequency. Appropriate circuits are being chosen from standard millimods and boards or developed as required. Design will be completed within the next quarter; no breadboard will be required.

O. Mechanical Design

The overall layout of the High Frequency Stimulus Rack was revised to correspond to the latest electrical design (see Figure 6-15).

Mechanical design of the units for the developmental model has started. During the next quarter, mechanical design, fabrication, and procurement of all detail parts should be completed. Assembly of the subchassis should be started.

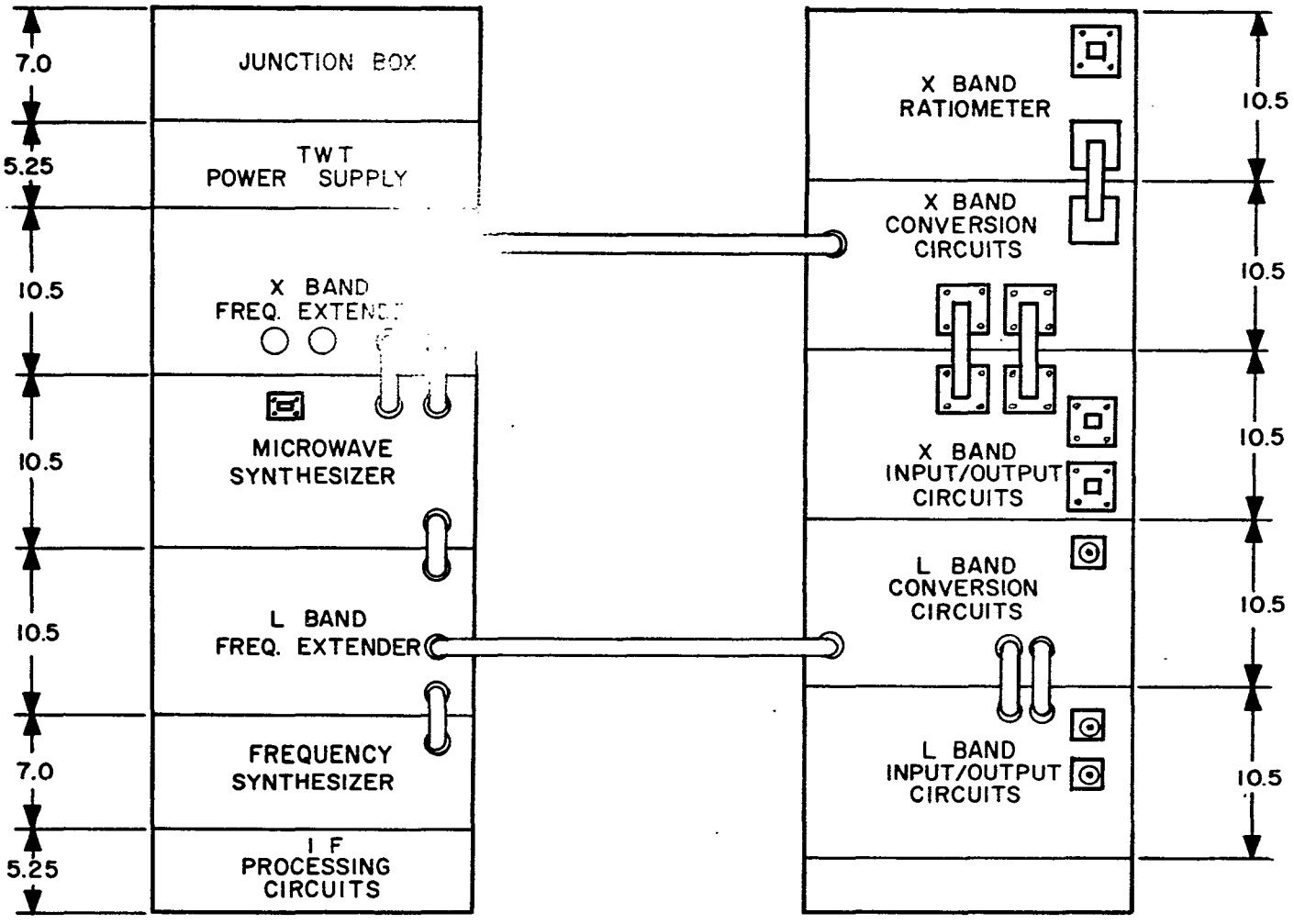


Figure 6-15. High frequency stimulus-rack layout

P. YIG Filter Development

Because the yttrium-iron-garnet (YIG) magnetically-tuned filter will not be required for MTE due to the unanticipated high sideband rejection obtained in the SSB modulators, their development has been discontinued, except for a cursory examination of models which were ready for test.

As previously reported several parallel approaches to YIG filter design were pursued.

a. X-Band YIG Filters (8-12 Gc)

The following types have been previously reported upon:

(1) In-line joint of crossed waveguides

(2) Strip transmission line - 90° phase-shift model

(3) Coaxial loop model

(4) Strip transmission line loop model.

All of the above types have been completed and tested. Results of tests on models of the second, third, and fourth types were unsatisfactory. The third type had a 3 db bandwidth of 1000 Mc, much too large for MTE. This model has been redesigned for use at L band.

The first type showed test results that meet or exceed most system requirements. Summary of test results follows:

Insertion loss: 1 db
VSWR: 1.5:1 (at pass band)
Bandwidth (3 db): 10 Mc
Offband rejection: 15 db @ $\pm$ 30 Mc; 30 db @ $\pm$ 200 Mc
Power handling capability: 100 HW milliwatts Average Power

During the reporting period, this model has been modified to reduce the air gap by 27%. An additional modification, to be completed early in January, will reduce the air gap to 0.200 inches, or a total reduction of 86%. This will permit a reduction in electromagnet power from 450 watts to 5 watts. Since orientation of the YIG sphere in the plane of the magnetic field will permit cancellation of YIG temperature-dependent terms in the frequency versus magnetic field relationship, a modification has been designed to permit this adjustment. This model is satisfactory for the MTE application; it will not be used, however, because the waveguide system described in paragraph 6.1.2 above meets the system carrier and unwanted sideband rejection specification without additional filtering.

Three other designes for an X-Band YIG filter have been investigated as follows:

(5) Crossed-waveguide coupler
(6) Pole piece in-line joint of crossed waveguides
(7) Waveguide below cutoff

The first of these three types employs the principle of a normal cross-waveguide coupler, wherein energy is coupled from one guide to the other through a coupling hole at a point of mutual circular polarization. (See Figure 6-16) Without a YIG sphere in place, and with the proper magnetic field impressed perpendicular to the axes of the waveguides, coupling much greater than that obtained without the YIG sphere installed is obtained. The model has been completed, but test results are inconclusive. At present, insertion loss is unacceptable, but a program of variation of YIG junction parameters is being carried out.

The second of the above three types employs the same principles as the first one, except that waveguide runs are integral with electomagnet

pole pieces. This technique eliminates the E plane bends close to the YIG junction, and is expected to produce a lower insertion loss and vswr at resonance than the first of the tree types. The air gap may be reduced to 0.100 inches in this model. Delivery of the completed model was made in late December. Test results showed this model to be a satisfactory solution. Power consumption was low (8 watts maximum at 12 Gc). In this configuration the magnetic field has a saddle shaped inhomogeneity caused by the mutually perpendicular waveguide aperture; this inhomogeneity has been shown to be sufficiently small that operation of the filter is not adversely affected. This model would be satisfactory for MTE use.

A possible third approach,if additional Q becomes necessary,utilizes the principle of a waveguide below cutoff to achieve off-resonance isolation (see Figure 6-17). The input and output lines are connected by a short section of highly cutoff waveguide into which two YIG spheres are introduced. The degree of coupling at ferrimagnetic resonance is controlled by the size and spacing of the crystals. The magnetic field is impressed perpendicular to the cutoff section.

An X-Band electromagnet has been designed to meet the programming unit power requirements. This unit has a designed air gap of 0.200 inches and may be used by all X-Band models. The reduction in airgap eliminates the problem of magnetic field drift because of coil heating, and leaves only those problems resulting from iron hysteresis and external ambient temperature changes. Delivery early in January is expected.

b. L-Band YIG Filters (1-2Gc)

Design modifications were made in the coaxial filter unit for use at L band, and these modifications areexpected to be complete early in January.

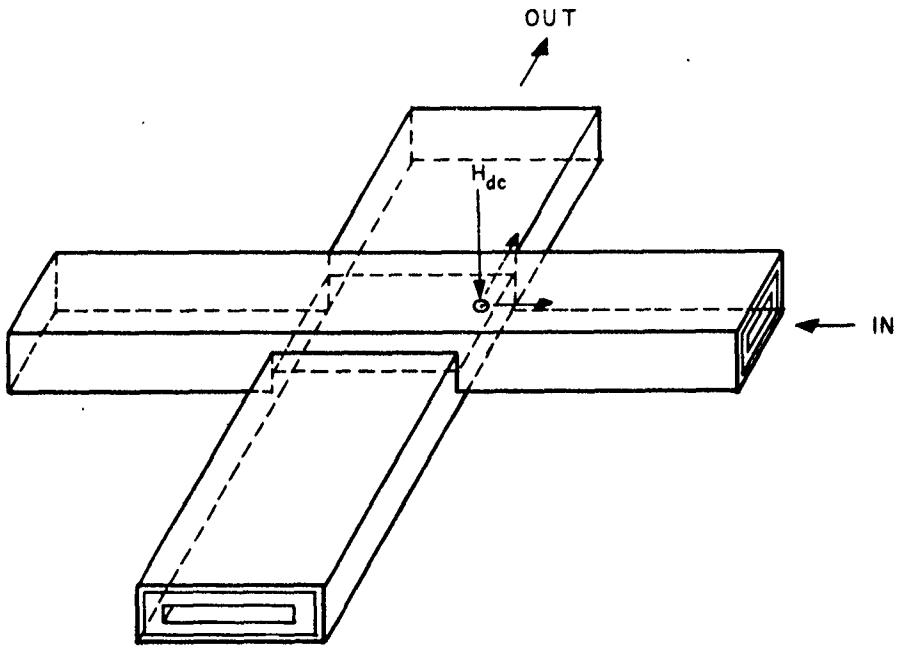


Figure 6-16. YIG filter-crossed waveguide type

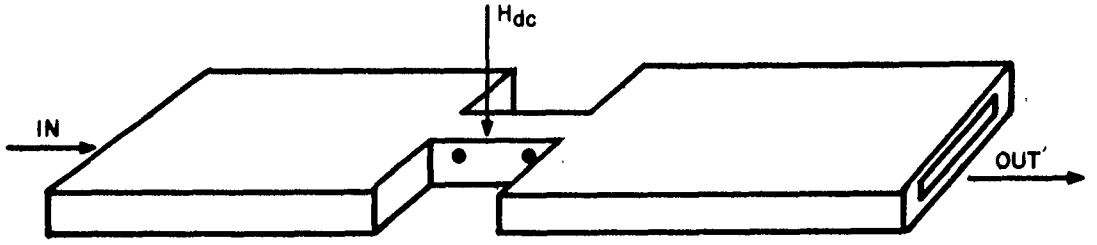


Figure 6-17. YIG filter - 2 stage high cut-off waveguide type

These modifications permit orientation of the YIG sphere in a plane containing the magnetic field, thus permitting cancellation of all YIG temperature-dependent terms in the frequency versus magnetic field relationship.

A second coaxial approach is available for use at L-Band if necessary. It utilizes the principle of two orthogonal coaxial lines connected by a hole which is well below cutoff (see Figure 6-18). With a YIG sphere in this coupling aperture, at ferrimagnetic resonance the magnetic field in the input line causes the magnetic moment of the YIG to precess about the applied dc magnetic field. This produces a component of magnetic field which couples to the output line. The zero field isolation (off-resonance) and insertion loss are controlled by the size of the coupling hole.

A gallium substituted YIG sphere will be used for L-Band, since pure YIG saturates magnetically below 3.5 Gc and is imperative below 1.7 Gc.

It has been concluded that neither coax design is required; if one is needed, the first of the two types would be used.

c. YIG Filter Power Supply

The theory of YIG filters can be found in the reference literature.[1, 2] The passband frequency is given by

$$f_r = K\phi$$

where K = constant

and ϕ = magnetic flux at YIG sphere

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1. Philip S. Carter, Jr., "Magnetically-tunable microwave filters, IRE TRANS. MTT, VOL. MTT-9, PP-252 - 260, May, 1961.
2. C. N. Patel, Mahnetically Tunable Filters, IRE TRANS. MTT, VOL. MTT-10, PP-152-161, May, 1962.

If the air gap is sufficiently wide that its reluctance is many times greater than that of the ferrous magnetic path,

$$\phi = K_1 I$$

where I = current in YIG electromagnet

so that

$$f_r = K_2 I$$

YIG filter tuning is accomplished in two steps: coarse tuning and fine tuning. For coarse tuning, circuit of the type illustrated in Figure 6-19 is being considered. It is easily shown that for large values of G,

$$I_o = \frac{V_F}{R_F} = \frac{V_R}{R_F}$$

The resistor R_R is digitally programmed, and f_r is brought to within a few megacycles of the required frequency. A servo loop is then used for fine tuning. A simplified diagram of the loop is shown in Figure 6-20.

The reference oscillator modulates the YIG control current, resulting in modulation of the rf signal which will be in phase or out of phase with the input voltage, depending upon whether its frequency is high or low (see Figure 6-21).

The error signal (i.e., crystal detector output) is amplified, phase-detected, and applied to the YIG filter. No significant difficulty is anticipated with this circuit.

A disadvantage of the servo tuning circuit is that modulations are produced on the output rf signal. By keeping the frequency within the passband of the microwave regulator, amplitude modulation will be removed. Frequency modulation may, however, still be present; their

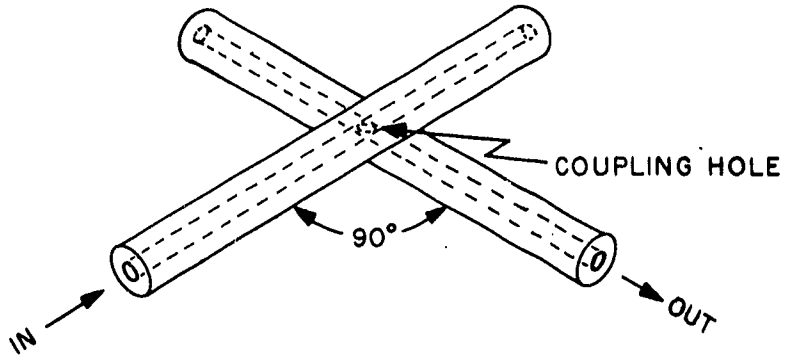

Figure 6-18. L-band YIG filter

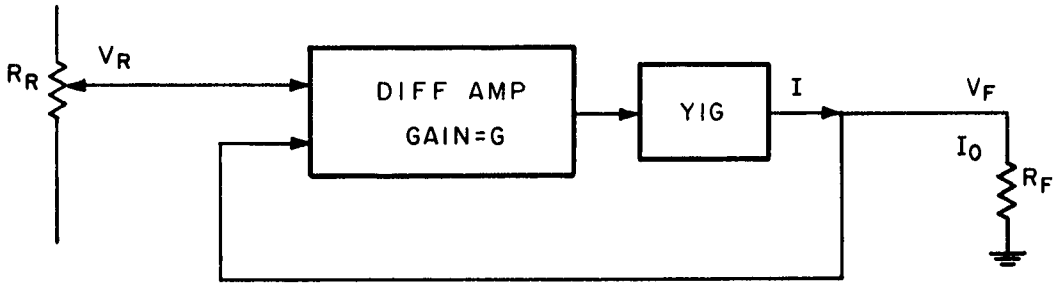

Figure 6-19. YIG filter current supply - coarse tuning

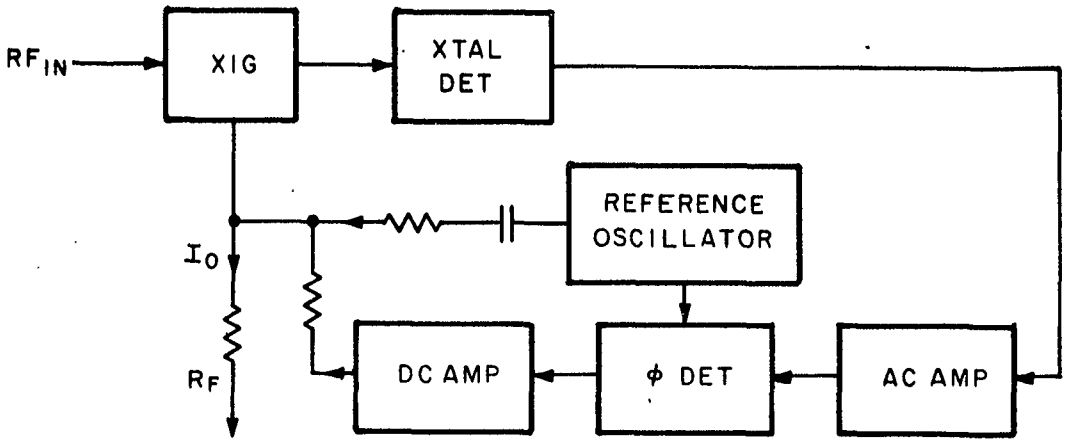

Figure 6-20. YIG filter fine tuning circuit

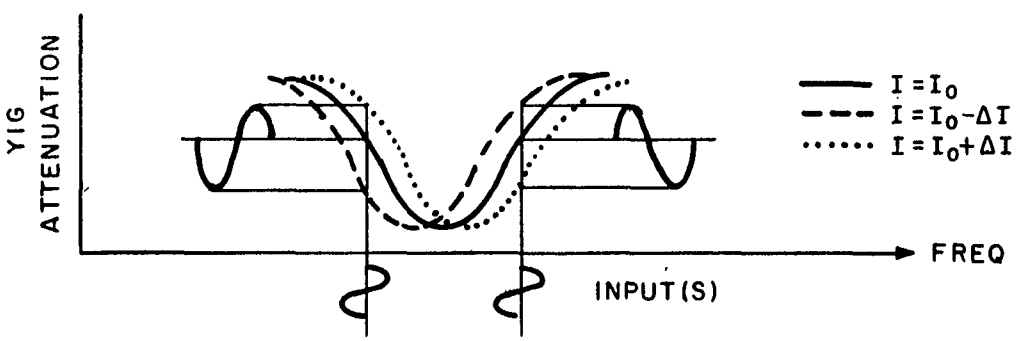

Figure 6-21. YIG filter passband characteristics

probable magnitude is determined as follows. If the YIG filter is equivalent to a reactance type wavemeter, the fm components will be of the form

$$f_{(t)} = A \sin \left| \omega_o t + (M \sin \omega_r t) \right|$$

where M = Modulation index

and ω_r = YIG modulation angle velocity

$= 2\pi f_r$

It can be shown that for phase modulation:

$$M = \frac{\Delta f}{f_r} = \frac{\Delta \theta f_r}{f_r} = \Delta \theta$$

Furthermore, the ith sideband is located at $f_o + if_r$ (i = 1, 2, 3, --) and is of relative amplitude J_i (m) (where J_i (m) is a Bessel function of the first kind).

Now J_1 (m) = m/2 - m3/16 +. . .

J_2 (m) $\approx$ m2/8 - . . . .

J_3 (m) $\approx$ m3/48 - . . . .

For a typical case, one may assume that m = 1/4 radians, hence the relative amplitudes of the sidebands are

J_1 (m) $\cong$ 1/8

J_2 (m) $\cong$ 1/128

J_3 (m) $\cong$ 1/3.100

J_4 (m) $\cong$ 1/100,000

The sideband energy will be confined to $f_o \pm 100$ cps for a 20 cps maximum expected modulation rate. The MTE specification permits deviations of up to but not including 2 kc; hence, the resulting fm will be well within specifications.

6.1.3 LOW FREQUENCY STIMULUS

Figure 6-22 shows the simplified block diagram of the Low Frequency Stimulus Group. There were no major design changes during this reporting period. All blocks shown are associated with the Electronics Test Units, except for the 115/10V. ac block which is associated with the Hydraulic Test Unit.

Paragraphs 6.1.3.1 through 6.1.3.17 describe progress and plans for the individual assemblies of the Low Frequency Stimulus Group, shown in Figure 6-22.

A. Very Low Frequency Generator

Figure 6-23 shows the block diagram of the Very Low Frequency Generator.

All basic control functions were determined and the preliminary logic design was completed. Standard MTE millimodules have been selected, except for the nonlinear resistor voltage divider and a part of the DACON. Values for the nonlinear resistor were chosen, and the DACON configuration was determined.

During the next quarter the final logic design will be completed. Design and test of the circuit to produce the nine internal frequencies from 1 to 9 Mc (which are used in developing the desired output very low frequencies) will complete overall circuit design. Since standard MTE circuits constitute most of the circuitry for the Very Low Frequency Generator, breadboard effort will be limited to nonstandard circuits. The Very Low Frequency Generator will be released to manufacturing during the next quarter.

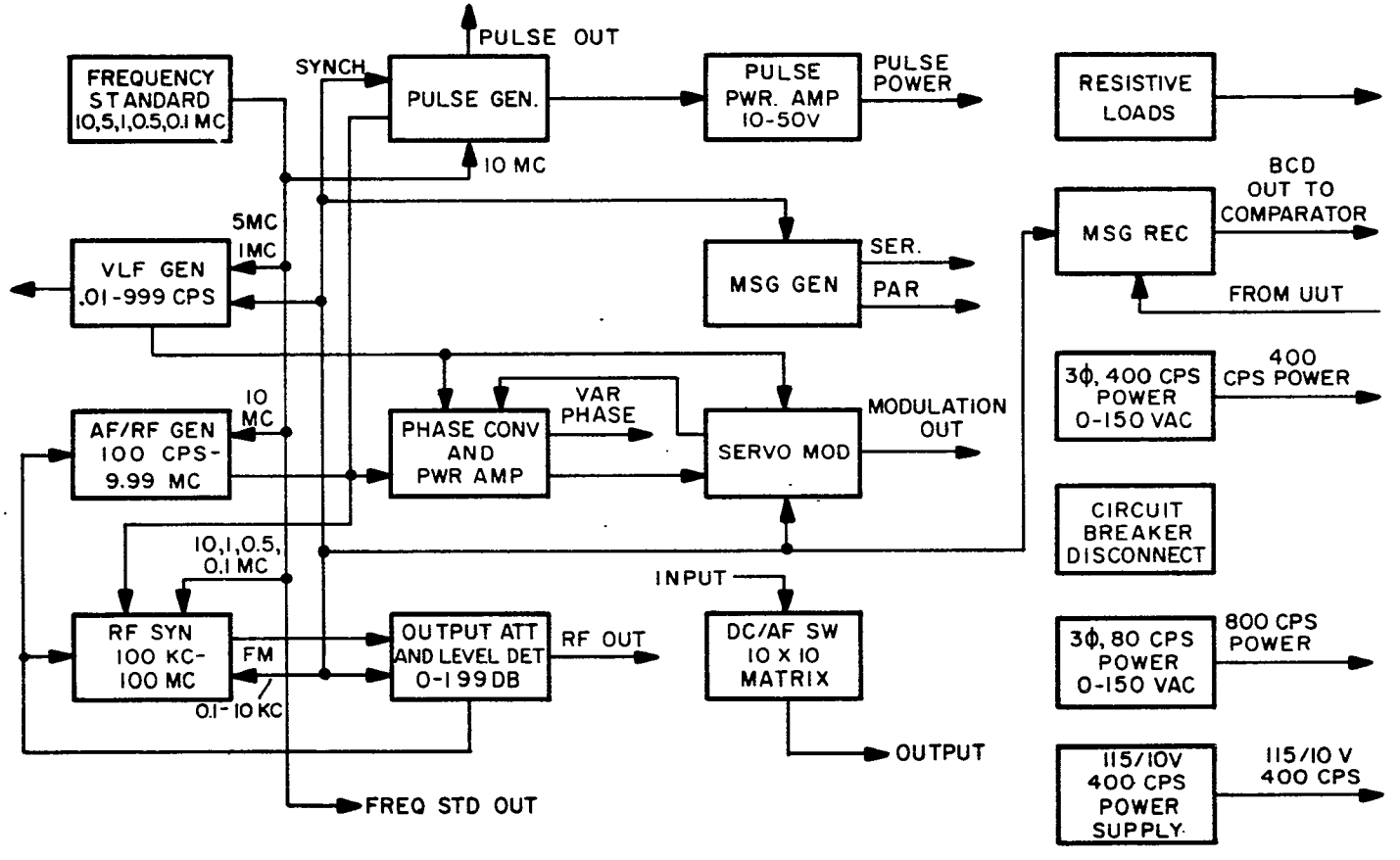

Figure 6-22. Low frequency stimulus - simplified block diagram

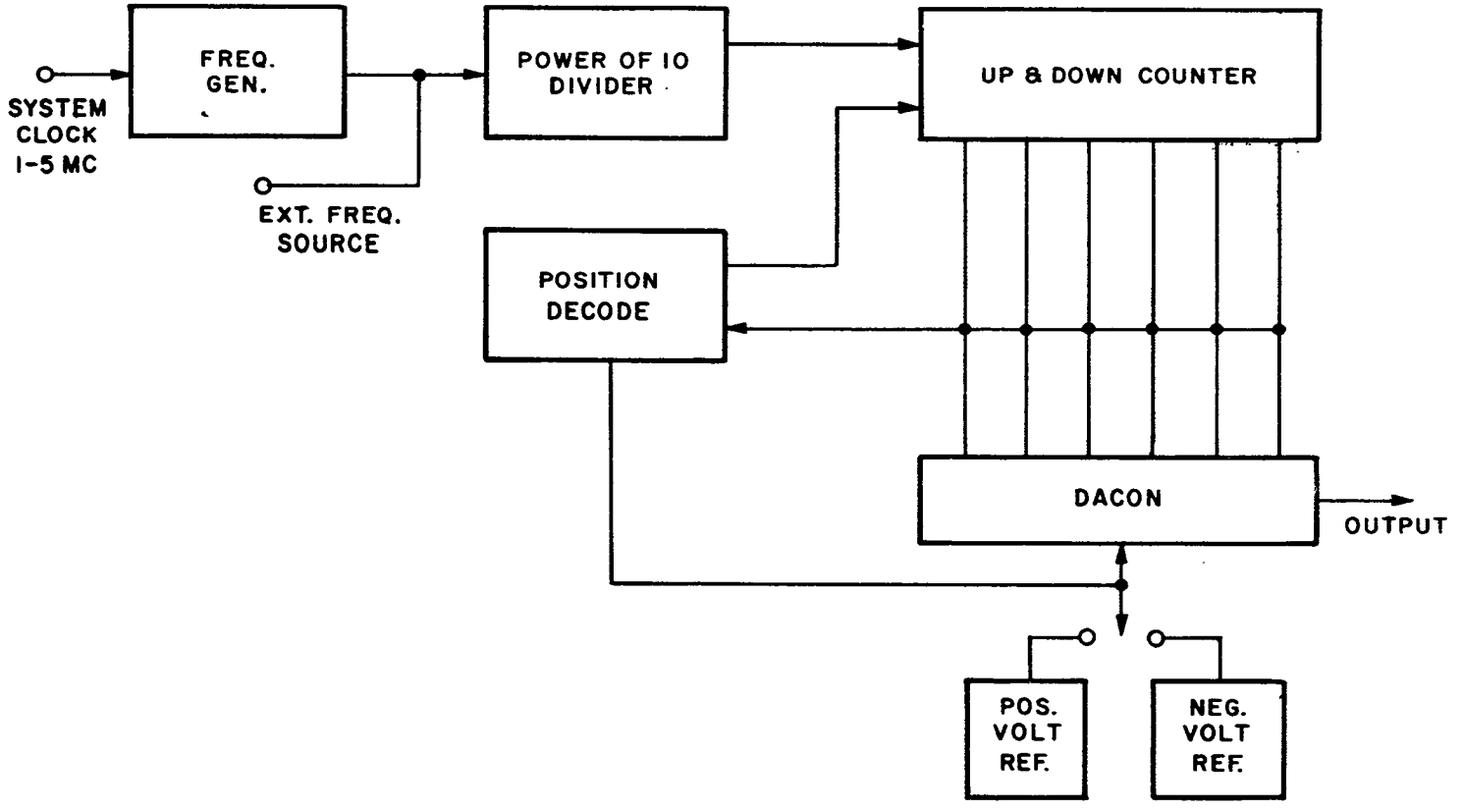

Figure 6-23. VLF generator - block diagram

B. AF/RF Generator

Figure 6-24 shows the block diagram for the AF/RF Generator. Frequency range of this unit is 100 cps to 9.99 Mc rather than 1 kc to 10 Mc as stated in the previous Quarterly Report.

Logic design and timing diagrams to check this logic were started. Standard MTE millimodules are used except for the VFO, filters, leveller, and a part of the DACON. It is probable that the DACON will be a modification of the DACON being developed for the VLF Generator.

Circuitry for the VFO is being investigated. Calculations show that a design to cover a 2 to 1 frequency range (5 to 10 Mc) would involve three frequency ranges to obtain the desired overall range. An alternate approach being considered is to design the VFO for a 15 to 20 Mc range and heat the 10 Mc standard with it to obtain the desired 5 to 10 Mc coverage.

During the next quarter the logic design will be finalized. Investigation of VFO circuitry will continue; the VFO and its associated DACON will be breadboarded. The output buffer and filters will be designed, breadboarded, and finalized. Overall electrical design will continue through the coming quarter, and will be completed in the second quarter of 1963.

C. RF Synthesizer

Figure 6-25 shows the RF Synthesizer in block diagram form. The work during the quarter, as described in the following paragraphs, covered all of the blocks shown except for the mixers following the 1 Mc and 10 Mc harmonic generators, the 370-460 Mc phase-locked loop, and the final mixer and output stage.

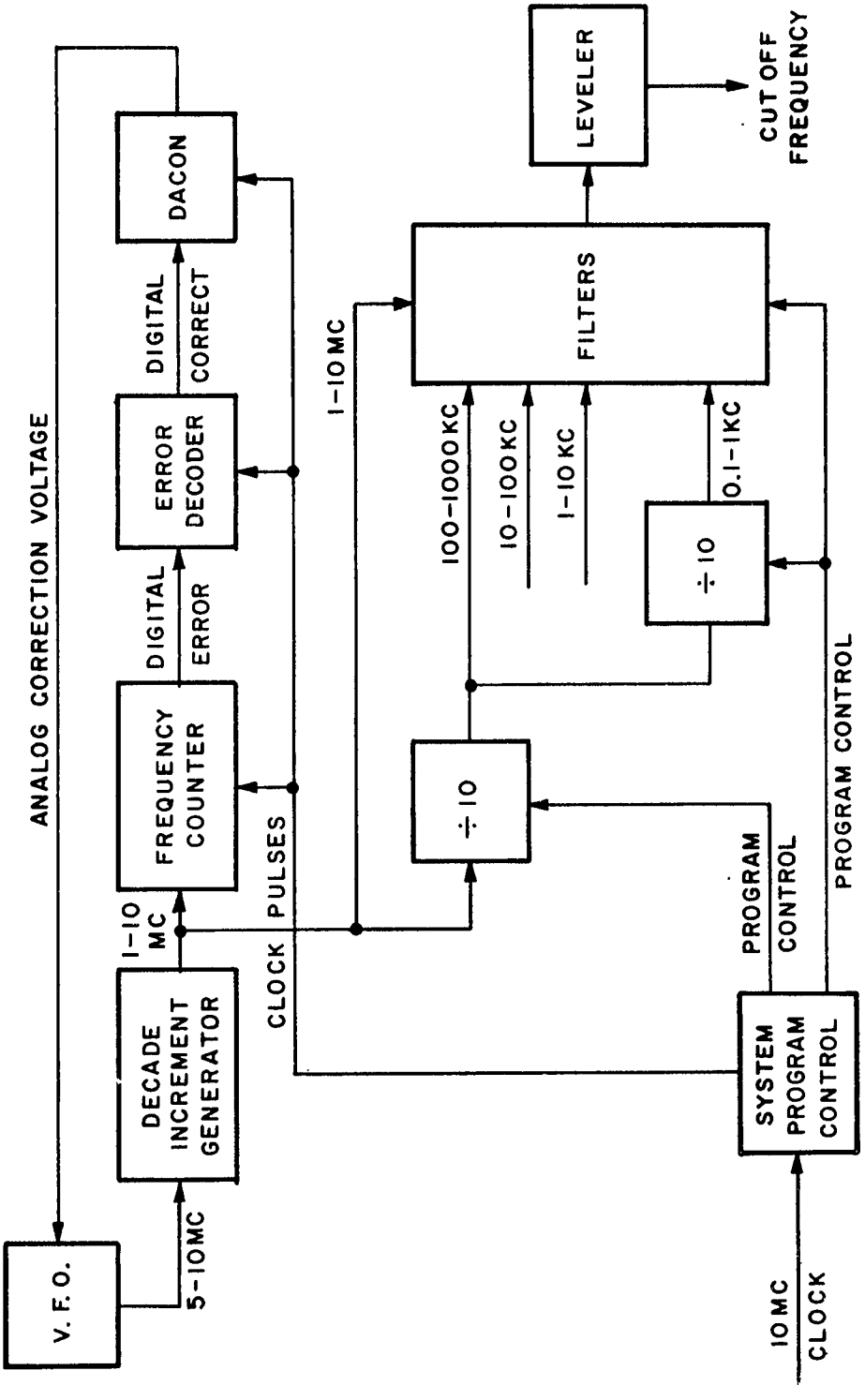

Figure 6-24. AF/RF generator-block diagram

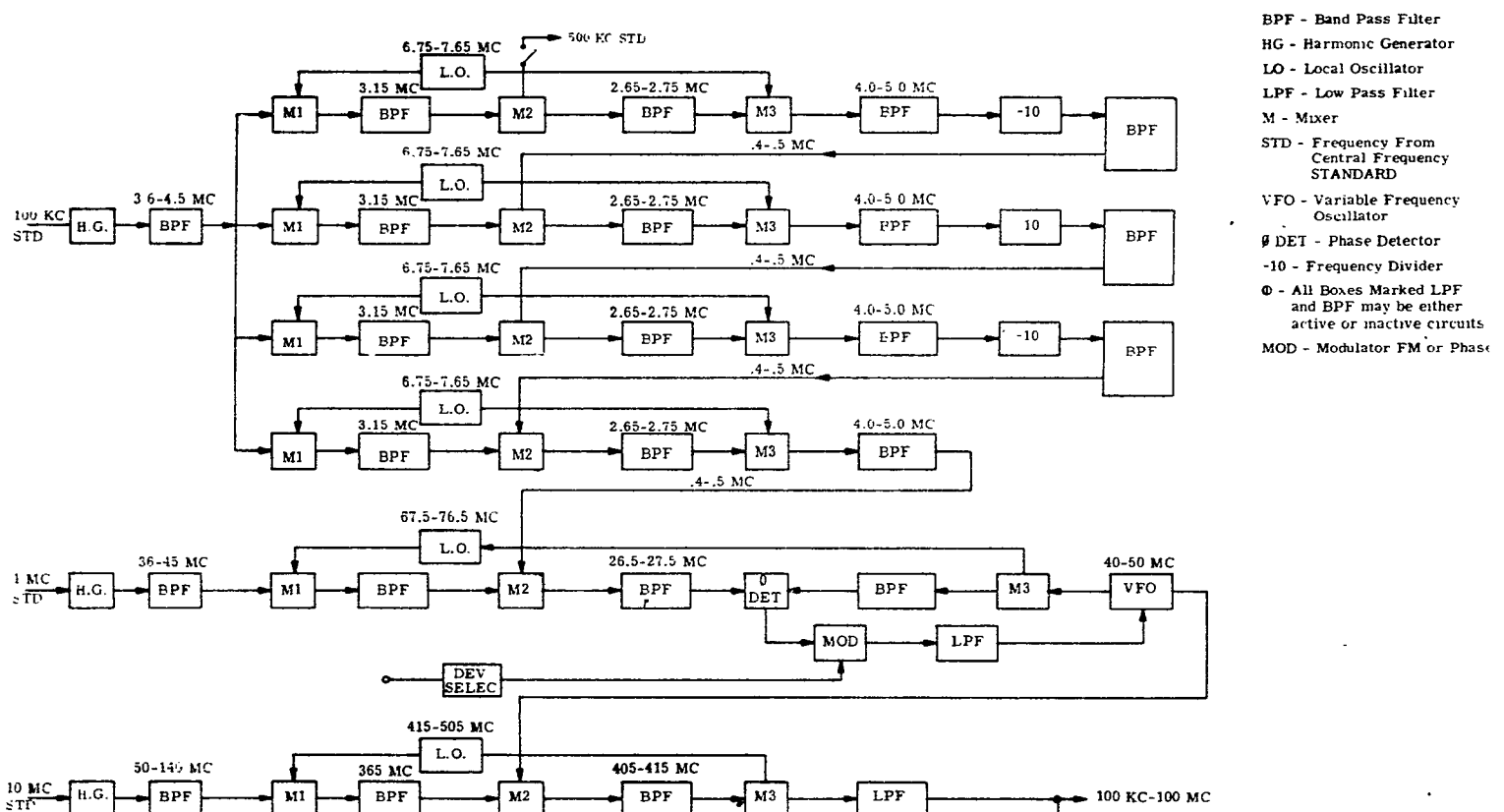

Figure 6-25. 100 kc - 100 Mc synthesizer - block diagram

a. Harmonic Generators

With respect to the 100 kc harmonic generator, a train of 100 kc pulses may be obtained from an avalanche circuit or from a monostable circuit using conventional transistor operation. Since it has been calculated, assuming a rectangular pulse, that the optimum pulse width is about 100 nanoseconds, a monostable circuit will be used. A circuit was designed and tested over a temperature range from -20 to +70°C; results were satisfactory. The associated -3.6 to 4.5 Mc bandpass filter was designed, breadboarded, and tested at room temperature; results were satisfactory. Release of this harmonic generator to manufacturing is scheduled for the second quarter of 1963.

For the 1 Mc harmonic generator, an avalanche circuit was developed and output was measured using a spectrum analyzer. The circuit included a bandpass filter of preliminary design. Harmonic content varied over the band of interest (35 Mc to 45 Mc) due largely to filter response; this will be improved in the final design of the filter. The harmonics will be amplified by a bandpass amplifier before being passed to the mixer circuit. Completion of design of this harmonic generator will be accomplished during the next quarter.

Pulses for the 10 Mc harmonic generator have been measured using a sampling oscilloscope. The harmonic content will be measured after the appropriate bandpass filter is designed. Completion of design of this harmonic generator will be accomplished during the next quarter.

Overall design of the above three harmonic generators and their associated bandpass filters will be completed during the second quarter of 1963.

b. Mixers

Mixer development effort during this quarter was confined to mixers associated with the 100 kc harmonic generator. The general requirements were to handle signals of the order of 5 to 10 milliwatts in range of 3 to 10 megacycles, without tuning, and with sufficient carrier suppression. The simplest circuit is the conventional balanced modulator. Several types of high speed high conductance diodes were examined and evaluated; the 1N914 silicon diode was selected for use in the circuit.

Investigation of broadband balanced transformer techniques led to the selection of Ferroxcube IIIC material for the magnetically closed core and Tape Cable Corporation S309 winding material. This material consists of three copper tapes sandwiched between two polyester films. Six turns of this material on the core formed the transformer windings, the center tape being the primary, the outer tapes the two half secondaries. The resulting transformer has excellent balance and is readily reproducible. Based on this transformer and the 1N914 diodes, the mixer circuit was designed and constructed, and initial testing started.

During the next quarter evaluation of the mixer design, covering carrier suppression and insertion losses for reactive terminations, will be completed. Mixer development of decades will be completed; the 10 Mc decade will be purchased; the 1 Mc decade will be breadboarded.

Information available on synthesizer output circuit design suggests a distributed amplifier rather than a feedback amplifier. Breadboarding will take place during the next quarter; completion of design is scheduled for the second quarter of 1963.

c. Filters

The 3.15 Mc bandpass filter in the 100 kc decades requires a 3 db bandwidth of 20 kc, and 60 db attenuation at 180 kc. Although the 3 db bandwidth is large for a crystal filter at this center frequency, the local oscillator temperature stability characteristic dictates this bandwidth.

Specifications for the 3.15 Mc crystal filter were released to several vendors for bid. Specifications are identical to those for the 3.15 Mc filter with a 10:1 frequency ratio.

Bids have been received from two suppliers; response from other vendors is expected shortly. During the next quarter, a vendor will be selected.

All other filters in the RF Synthesizer will be LC type. Design of four of these will be completed during the next quarter; the remainder will be completed during the second quarter of 1963.

d. Local Oscillators

For the 6.75 to 7.65 Mc local oscillator a Colpitts circuit was chosen. LC tank circuit components were chosen compatible with a standard varicap, tested for bias voltage range to cause least temperature variation error.

In the design of the biasing network, consideration was given to transistor temperature stability. The tank circuit will have two variable components - inductor and trimmer, employed for two point tracking to allow for variations between varicaps. The 100 kc steps required from the oscillator will be programmed by variation of varicap bias; the entire frequency range can be achieved with a range of 15 to 50 volts.

The following breadboard tests were performed: (1) the effect of 10% change in supply voltage; (2) the effect of wide changes in load resistance; (3) the substitution of different varicaps with some manufacturer's designation; and (4) varicap voltage versus frequency. Results of the first two tests (design verification) were satisfactory. The third test showed that, with bias voltage held constant, the LC tank circuit variables could be adjusted to obtain the same oscillator frequency with different varicaps. The fourth test showed that the frequency vs. voltage characteristic could be closely approximated by two linear segments; a circuit modification may make this characteristic linear, simplifying the design of the DACON which supplies the varicap voltage.

During the next quarter data will determine oscillator stability obtainable with temperature compensating components; the circuits will be finalized.

The 67.5 to 76.5 Mc local oscillator will employ essentially the same circuit used for the 6.75 to 7.65 Mc oscillator. The transistor will require a larger gain-bandwidth product, hence the 2N918 was chosen. The same varicap and voltage range will be used. Consequently, an inductance 1/100 that employed in the lower frequency oscillator can be used. During the next quarter the circuits will be finalized. Release to manufacturing is scheduled for the second quarter of 1963.

General requirements have been established for buffer amplifiers which follow the local oscillators. During the next quarter, circuit design will be completed, and the buffers will be released to manufacturing.

e. 10:1 Dividers

A four-stage binary counter and the standard MTE flipflop will be used. During the next quarter the boards will be laid out and design check-out started. Release to manufacturing is scheduled for the second quarter of 1963.

f. 360-370 Mc Phase Locked Loop

The 40-50 Mc phase detector is a balanced bridge type, chosen over a full wave type because it can drive a considerably lower load impedance, 100K vs. 1 meg or greater.

A driver amplifier which provides the 40-50 Mc signal voltage to switch phase detector diodes is working in breadboard form.

Because of the large signal required into the detector from the VFO, an additional driver will be used.

The 360-370 Mc VFO has been designed and is being breadboarded. All parts have been ordered. The oscillator is a common emitter configuration with the feedback supplied to base of a 2N917 transistor which has a F_T of 800 Mc. The 2N917 was chosen primarily because of the large gain-bandwidth product and low output capacitance. The voltage-variable capacitor chosen to tune the oscillator is a Pacific Semiconductor PC-115-10 which is equal to 10 Pf at 4 volts. The voltage tuning range is 15 volts at 360 Mc to 17.7 volts at 370 Mc. The sensitivity of the VFO at 15 volts varicap bias is approximately 4 Mc/volt. Two output amplifiers are being designed, one to supply the mixer in the closed loop feeding the phase detector, and one to provide a signal to the next 10 Mc closed loop. These amplifiers will use 2N917 transistors because of the high F_T. A buffer amplifier will be required between these amplifiers and the VFO.

General requirements for the mixer have been established; make or buy.

The 360-370 Mc bandpass filter will be designed into the VFO output amplifier. Characteristics depend upon the frequency spectrum of the output signal, detailed design will begin when a closed loop system is working.

Feasibility of frequency modulation in a closed loop system can be established when the closed loop is in operation. An alternative design approach is to frequency modulate the 320 Mc reference voltage injected into the mixer in the closed loop.

Except for the FM portion, the Phase-Locked Loop will be completed and released to manufacturing during the next quarter. The FM portion will be released during the second quarter of 1963.

g. 320 Mc Generator

The 320 Mc generator, which develops this frequency by multiplication of the 10 Mc standard signal, was designed, breadboarded and tested.

The circuit consists of a 2N706 transistor Class C doubler to 20 Mc, a shunt varactor doubler to 40 Mc, a 2N706 transistor Class C doubler to 80 Mc, a shunt varactor doubler to 160 Mc, and a shunt varactor doubler to 320 Mc.

Varactor multiplication greater than two was not attempted because of (1) poor efficiency and (2) complexity of tuning due to interaction between tuned circuits. Estimated overall gain of the three varactor stages is minus 10 db; estimated overall gain of the two transistor stages is 26 db. Shunt type varactor doublers were chosen in preference to the series type because the shunt configuration is capable of generating only the second harmonic.

Test results showed satisfactory operation through 160 Mc. Higher Q varactors are being investigated for 320 Mc to obtain better selectivity, harmonic suppression, and efficiency. A bandpass filter will probably be added at the 320 Mc output. Completion of design and release to manufacturing will be accomplished during the next quarter.

h. 370-460 Mc Phase Locked Loop

Major activity for this loop is scheduled for the second quarter of 1963.

i. Final Mixer and Output Stage

Major activity for these items is scheduled for the second quarter of 1963.

D. Frequency Standard

Figure 6-26 shows the Frequency Standard in Block Diagram form. Stability requirements for this unit changed as a result of the Test Requirements. Analysis is:

Long term stability: 1 part in 10^9 per 24 hours
Short term stability: 1 part in 10^9 per second

The change in stability requirements resulted in the decision to use a crystal-controlled standard manufactured by Motorola This standard offers the following advantages over those previously considered:

(1) Military qualified: used in the AN/USC-3(v)

(2) Weight: 14 oz

(3) Volume: 24 cubic inches

(4) Operating temperature range: $-55^{\circ}C$ to $+77^{\circ}C$

(5) Short warmup time

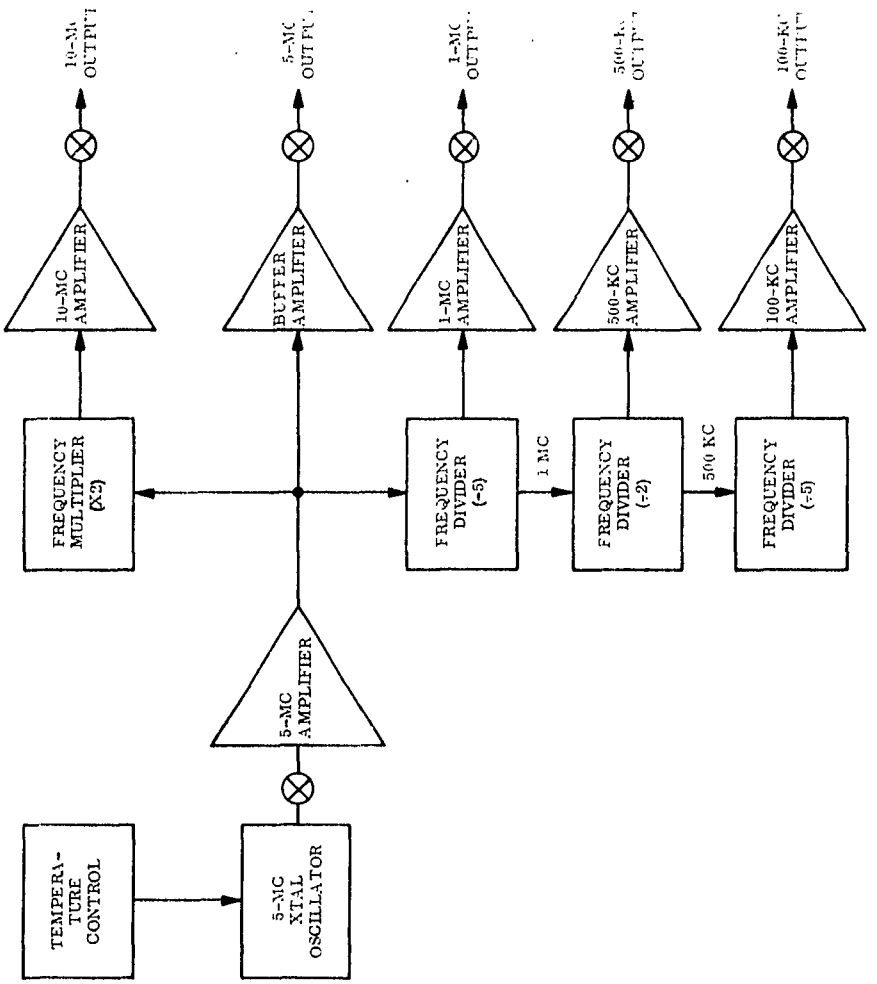

Figure 6-26. Frequency standard (5738) - block diagram

(6) Lower cost.

This unit does not require batteries for use as standby power as the James Knights model 1100 T does.

Preliminary circuit design for the multipliers and amplifiers was completed. The 1 Mc section was breadboarded and tested at room temperature with satisfactory results.

During the next quarter the multiply and divide breadboards will be completed, and the frequency standard released to manufacturing.

The following characteristics are supplied to supplement information given in the Second Quarterly Report:

Unit: Motorola Model SLN 6039 A
Crystal oscillator frequency: 3 Mc
Output frequency: 3 Mc
Weight: 0.88 lb
Volume: 0.014 cu ft
Panel height: 2.1 inches
Stability long term: 1 part in 10^9 after 30 hour warmup
Stability short term: 2 parts in 10^{10} per second
Output level: 0.2v into 1000 ohm load
Temperature: -55°C to 75°C

E. Output Attenuator and Level Detector

Figure 6-27 shows this unit in block diagram form.

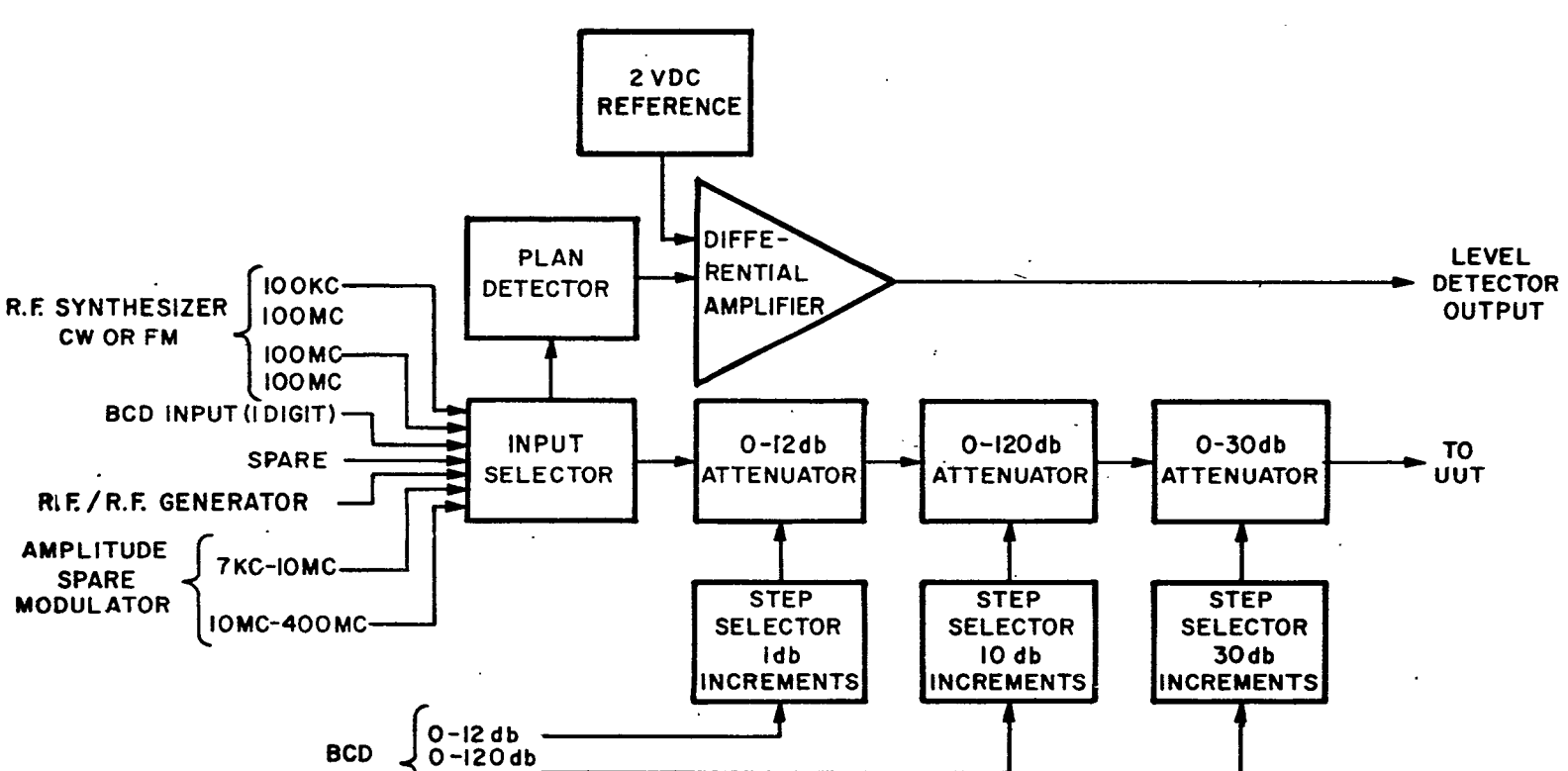

Figure 6-27. Output attenuator and level detector-block diagram

Two proposals have been received in response to requests for quote on the 0 to 199 db attenuator; additional technical and cost data are being solicited to enable a selection to be made in the next quarter.

The design and breadboard tests initiated during this quarter for a level detector are expected to be completed for release to manufacturing in the next quarter.

F. Pulse Generator

A polarity selection function has been added to the output control in the Pulse Generator.

Final logic diagram, started during this quarter will be completed. Breadboard construction and evaluation will be completed. Since the pulse generator will be built mainly with standard circuits, only the unique circuitry will be breadboarded.

G. Message Generator

One new feature was added; the output frame ratewill be determined by a clock signal received from the AF/RF Generator. Release to manufacturing is scheduled for the second quarter of 1963.

H. Message Receiver

The design was altered to make the input frame rate a function of the UUT. Release to manufacturing is scheduled for the second quarter of 1963.

I. Phase Converter and Power Amplifier

This unit is capable of phase-shifting and amplifying 40, 400 or 800 cps input signals, and providing output signals which are programmable

in amplitude and phase. The preliminary simplified block diagram is shown in Figure 6-28.

Initial circuit design of the phase shift networks and the power amplifiers is in progress. No problem areas are anticipated.

During the next quarter, breadboard fabrication and test of one of the three channels will be completed. Verification of one channel should prove the design, as the three channels are similar.

J. DC/AF Switching Unit

Parts were ordered for breadboard testing of the relay driver circuit, scheduled for completion during the next reporting period.

K. Resistive Load

Figure 6-29 shows the block diagram for the Resistive Load.

High current relay and relay driver samples have been ordered. Types and quantities of other relays required will be determined, and final design completed during the next quarter.

L. 400 cps Power Supply

This is a programmable regulated 400 cycle stimulus power supply. A circuit was breadboarded which demonstrated the feasibility of using silicon controlled rectifiers (SCRs) with phase control. Distortion was held to 5 percent maximum. Additional work will be done in the following quarter to eliminate residual instability at low output levels.

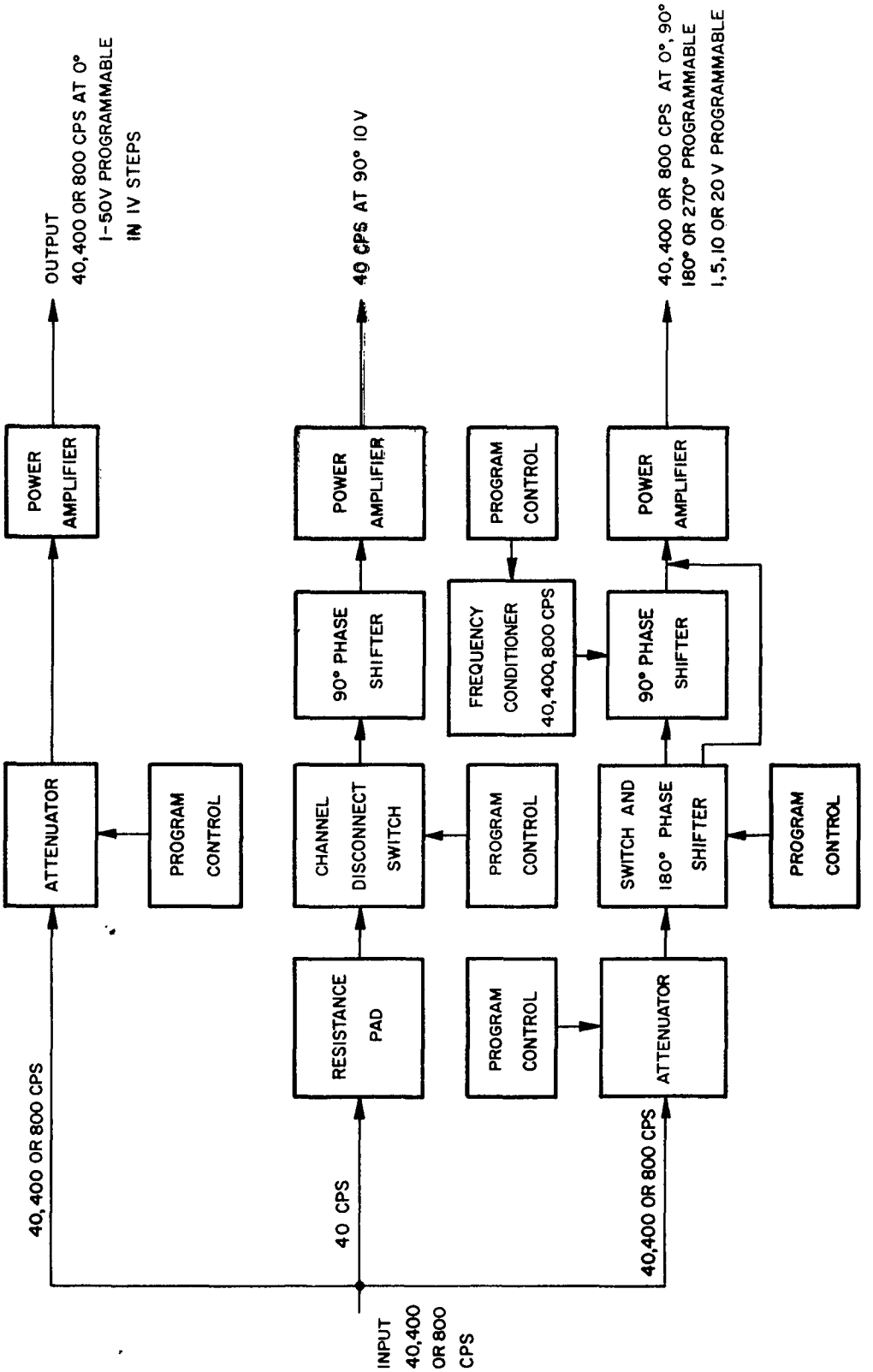

Figure 6-28. Phase converter and power amplifier - block diagram

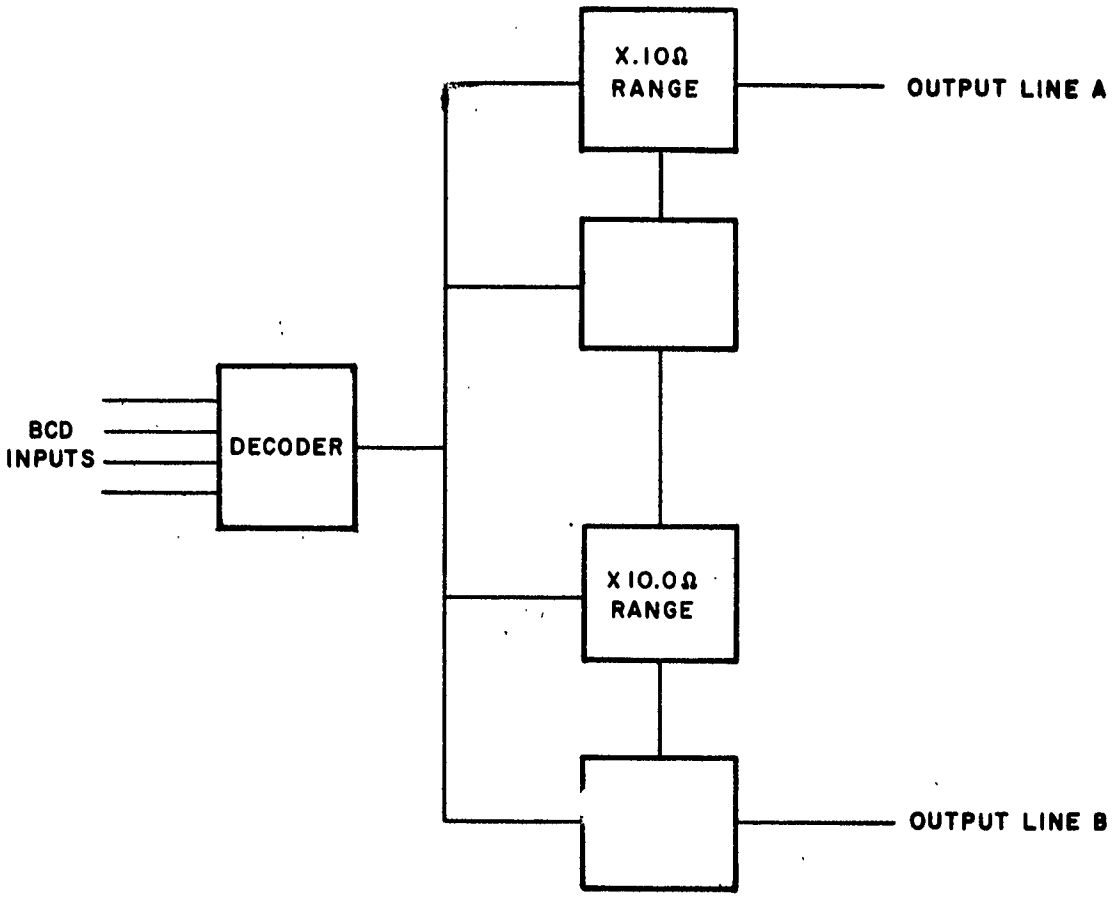

Figure 6-29 Resistive load-block diagram

M. 800 cps Power Supply

The output current of this supply will be 3 amperes per phase, rather than the 30 ampere figure indicated in the previous quarterly report.

This power supply uses essentially the same circuit as the 400 cps power supply, except for small changes in component values dictated by frequency difference.

During the next quarter one complete power supply (all three phases) will be breadboarded, and temperature and response tests performed, with control circuitry taken from the 400 cps breadboard.

N. Circuit Breaker Disconnect Unit

The preliminary electrical design was completed; during the next quarter, final design will be completed. No breadboarding is anticipated.

O. 115/10 volt AC Power Supply

This power supply required for the Hydraulic Test Unit, furnishes 400 cps single phase stimulus power programmable to either 115 or 10 volts, at rated full load current of 1 ampere. A tapped transformer will probably be adequate.

6.1.4 DC STIMULUS

The DC Stimulus Group is contained in one and one-half MTE standard racks (see Figure 6-30). The full rack is in ETU 2, the other rack in the Hydraulic Test Unit contains controller equipment in addition to the DC stimulus equipment.

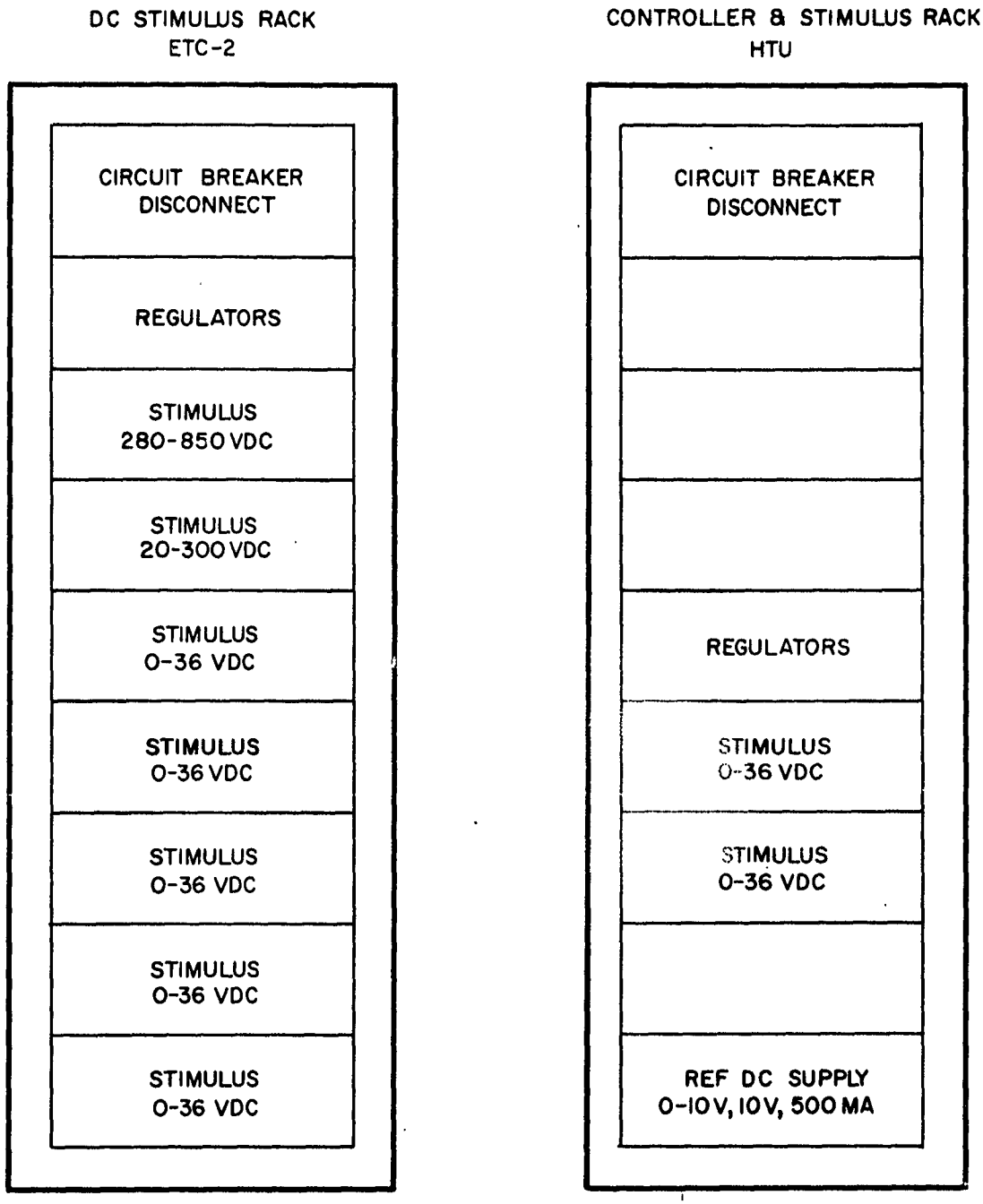

Figure 6-30. DC Stimulus rack layout

A. Progress During Quarter

a. Circuit Development

The DC Stimulus generators are of two types: those programmable down to zero and those programmable to some minimum voltage, such as 20 volts. The block diagram shown in the Second Quarterly Report applies to both, minor circuit changes allowing for the difference.

Each type circuit was designed, breadboarded, and tested (without the pre-regulation circuits) during the quarter. The pre-regulation circuits have been designed and are currently being assembled for integration into the balance of the circuits. It may be noted that the 0 to 9.99 volt supply does not require pre-regulation. Each generator is programmable by means of a relay-controlled resistor network. The logic design of the programmable networks is presently nearing completion.

b. Mechanical Development

A mechanical design for the DC stimulus assemblies was established during the quarter. Each generator is contained in an MTE standard chassis divided into two compartments, the left side containing the printed circuit cards and the right side containing the chassis mounted components as shown in Figure 6-31.

B. Plans for Next Quarter

During the next quarter it is planned to: (1) complete all electrical design and breadboarding: (2) complete all drafting: (3) release the DC stimulus group for part procurement and fabrication of the assemblies required for the MTE development model.

6.1.5 MEASUREMENTS

A. General

A simplified block diagram of the Measurements Group is shown in Figure 6-32. Each block was discussed in some detail in the Second Quarterly Interim Technical Report. Progress during this quarter is described with reference to the same diagrams reproduced and marked for convenience.

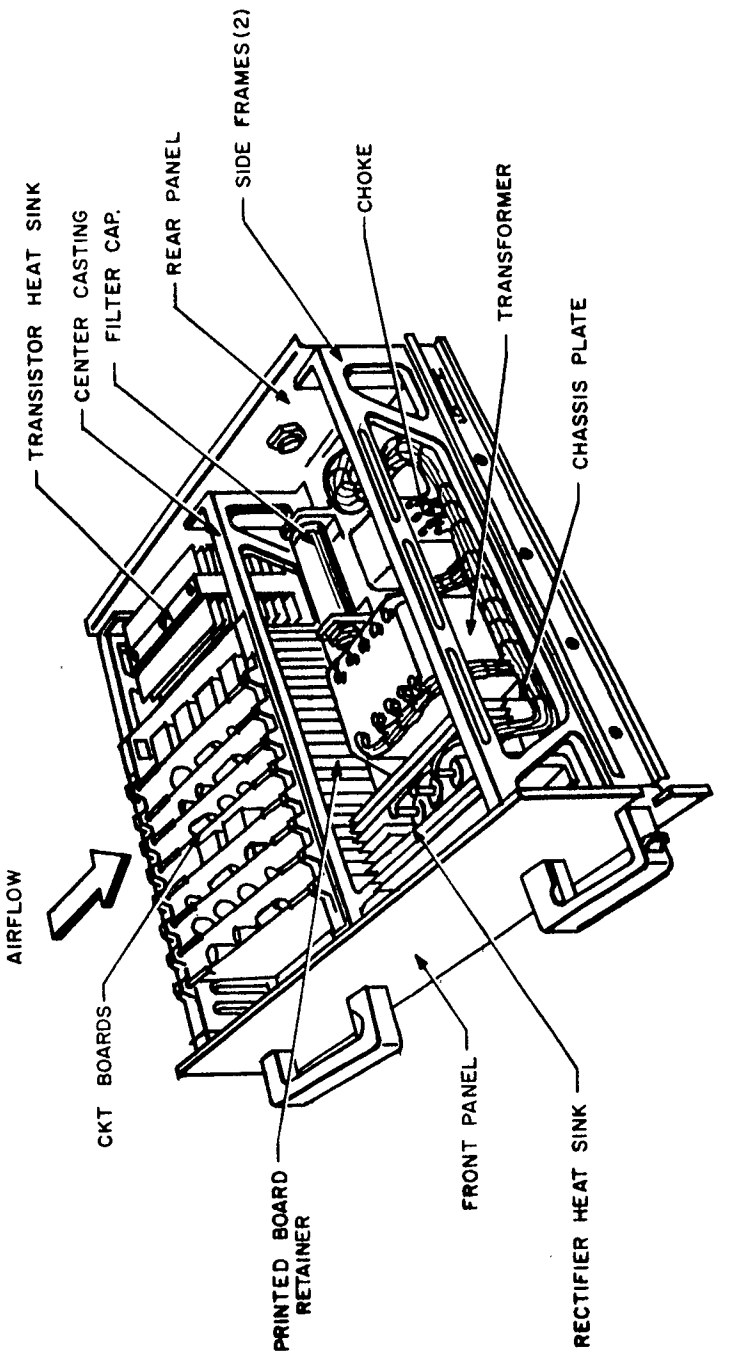

Figure 6-31 Typical DC stimulus chassis

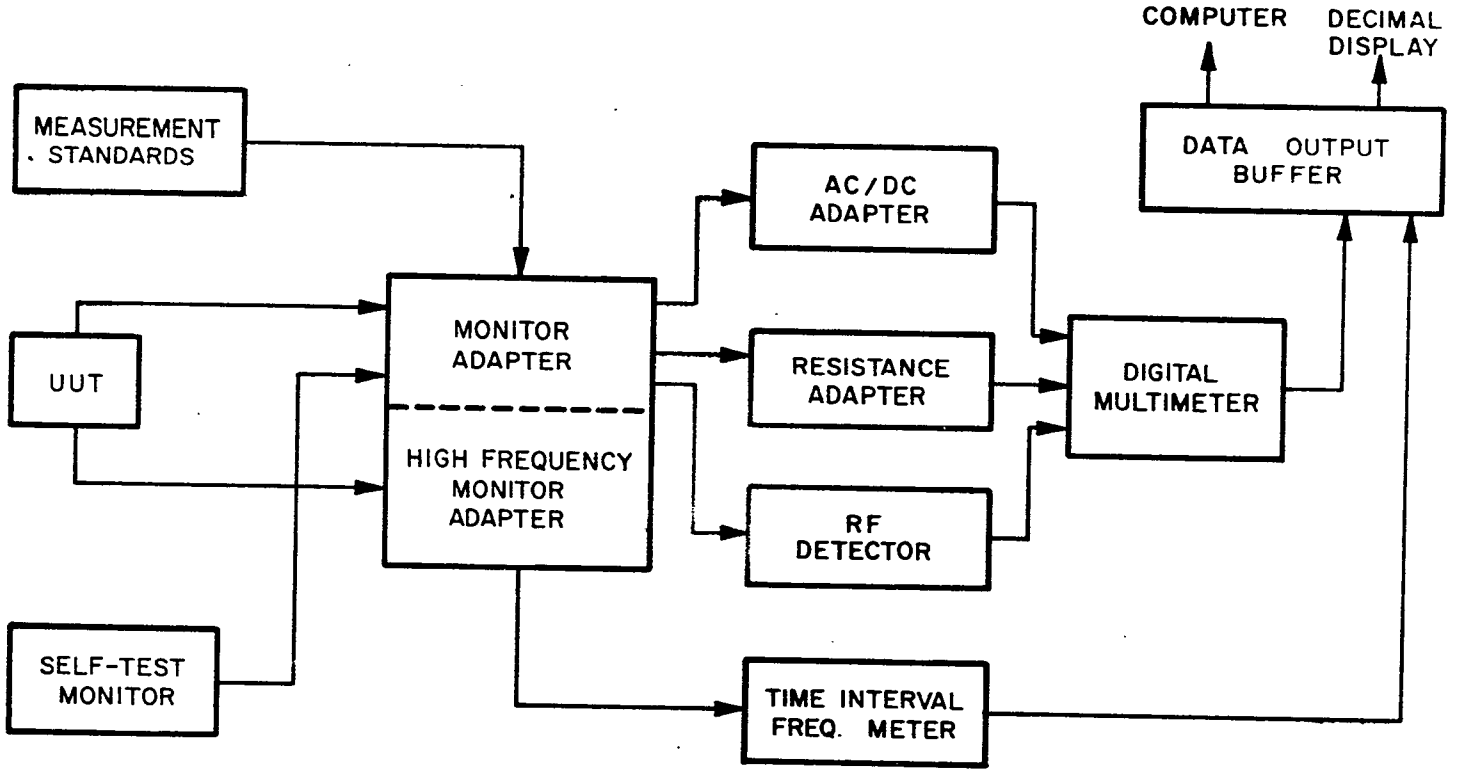

Figure 6-32. Measurements group - simplified block diagram

The design of this Group is nearing completion with release to drafting scheduled for early in the coming quarter.

B. Measurement Standards

Requests for quotation have been sent to prospective vendors of the ac and dc voltage standards; each standard will have a fixed output voltage in the range 5,000 to 9,500 volts.

Purchase orders for these and the resistance standard will be issued during the next quarter. Mechanical design of the standards assembly will begin with receipt of pertinent dimensions from selected vendors.

C. Monitor Adapter

The Logical design of the Monitor Adapter Unit was completed during this report period. The switching capability of the Monitor Adapter, described in the Second Quarterly Report, has been slightly altered. The present capability is as follows: For the A matrix, any one of 89 low frequency test points can be switched to the low frequency A output bus and any one of 10 coaxial test points can be switched to the high frequency A output bus. For the B matrix, any one of 79 low frequency test points can be switched to the low frequency B output bus and any one of 20 coaxial test points can be switched to the high frequency B output bus.

None of the test points is common to both matrices, they can be made so, however, by external connection. Either of the B output buses can be switched to the input of RF probe in the Monitor Adapter.

Monitor Adapter circuit development made satisfactory progress during the quarter. An "exclusive or" gate was built from standard components and successfully tested over the temperature range -25°C to +70°C. A

level detector to check the reed relays used in the relay gating and driving board was also designed, built and successfully tested.

Two reed relay boards of the five types of boards used in the relay matrix sections have been designed and released to drafting; block diagrams of the three other boards have been completed. The Monitor Adapter occupies 2-1/2 levels (drawers); the mechanical layout of one level is in process.

During the next quarter, drafting of the Monitor Adapter will be completed and released to production.

D. Self-Test Monitor

The logical design of the Self-Test Monitor was completed during this report period. The only change was an alteration of the switching capability. Any one of 30 low frequency test point pairs may now be selected, one test point of the pair is placed on the low frequency A bus and the other in the low frequency B bus. Any one of 4 coaxial test points may be selected and placed on the high frequency B bus. Either of the B output buses may be switched to the input of the RF probe contained in the Monitor Adapter.

Since the circuits used are the same as those used in the Monitor Adapter, status and progress is as described in Section 6.1.5.B. Mechanical layout of the 1-1/2 levels is well along.

During the next quarter, drafting of the Self-Test Monitor will be completed and released to production.

E. Time Interval Frequency Meter

The Time Interval Frequency Meter is reproduced in block diagram form in Figure 6-33. Major effort was devoted to the circuits and equipment between the vertical dashed lines on the Figure. The remaining equipment is largely composed of standard millimodule circuits; the logic for these standard circuits has been developed.

Breadboarded and tested during the quarter were:

(1) the Schmitt trigger

(2) the decade divider

(3) the time interval start-stop control, and

(4) the clock pulse amplifier (used to amplify the crystal clock output).

Quotes have been received on the long-lead items represented by the crystal clock and the amplifiers; orders will be placed early in the next quarter.

Remaining to be developed are circuits to drive the decade divider and the phase inverter portion of the time interval start stop control.

During the next quarter (1) all TIFM circuit development will be completed; (2) printed circuit boards will be released to drafting and then to production.

F. RF Detector

The design of the RF detector was established. A 1N3064 crystal diode was chosen, the circuit was breadboarded and tested for temperature changes and for performance variations due to tolerance of characteristics from unit to unit. The design has been released to drafting and will be released to manufacturing during the coming quarter.

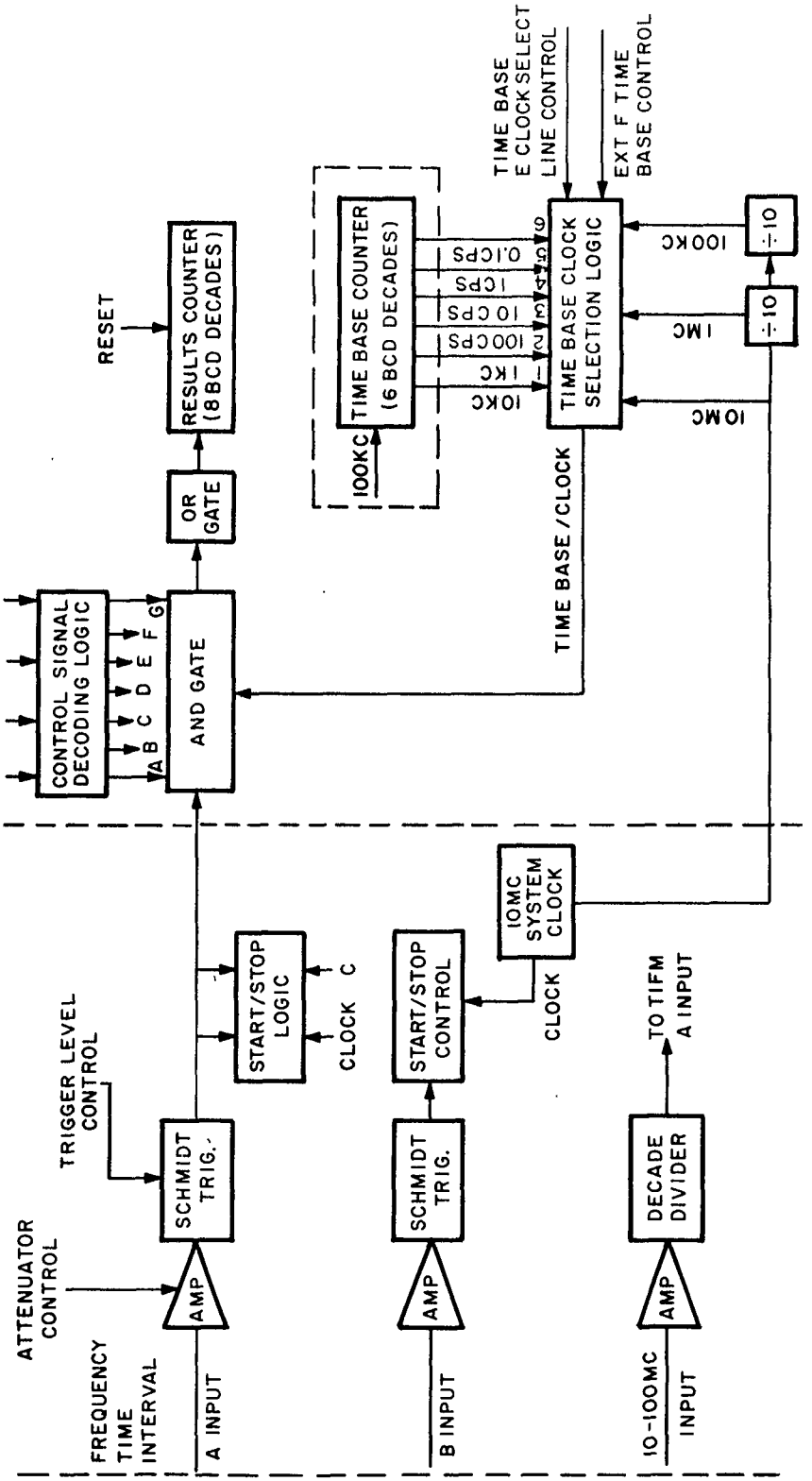

Figure 6-33 Time interval frequency meter

G. AC/DC Adapter

The requirements of the AC/DC Adapter were defined; make or buy decision will be determined early in the next quarter.

H. Resistance Adapter

Components are identical to those required for the AC/DC Adapter. Make or buy decision will be made early in the next quarter.

I. Digital Multimeter

The Digital Multimeter was described in the Second Quarterly Interim Technical Report. The functional block diagram is reproduced in Figure 6-34 to facilitate the discussion.

Effort was expended on the special circuits shown cross-hatched on the block diagram. Other items are standard circuits or purchased items and present no problems.

The chopper input circuitry was breadboarded and tested; although development is not yet complete, a satisfactory circuit is attainable with some refinement to the present circuit. The amplifier and shaper circuits following the chopper have been designed and breadboarded; preliminary testing indicates satisfactory operation.

The reference voltage supplies for the DACON network were designed and breadboarded. The differential amplifier portion of the supplies will have to be kept in a controlled temperature environment to keep output voltage drift within acceptable limits. The regulation and response of the regulator portions of this circuit are satisfactory.

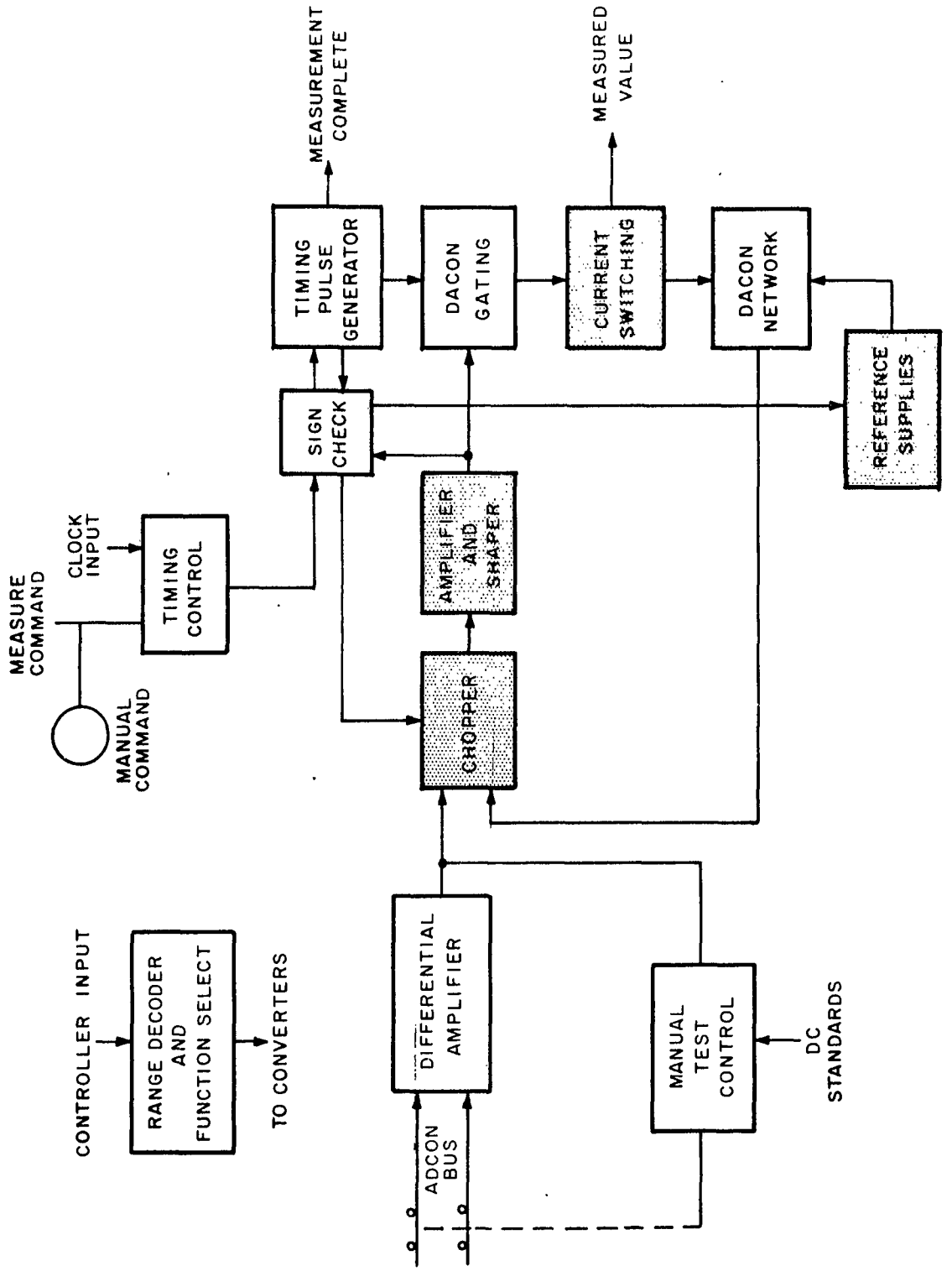

Figure 6-34. Digital multimeter functional block diagram

Techniques and devices to perform DACON current switching are presently under investigation. Low-loss switches are required for this application.

During the next quarter, all design for the Digital Multimeter will be completed; the equipment for the MTE development model will be released to drafting and then to manufacturing.

J. Data Output Buffer

The design concept described in the Second Quarterly Interim Technical Report has since been discarded as the space required is not available. To package the data output buffer in one standard MTE level an alternate approach has been taken in the area of input gating and control. Additional space saving has been accomplished through the design of a lamp driver circuit which also performs a logic function.

During the next quarter, the design of the Data Output Buffer will be completed and the layout of the printed circuit boards will be started.

6.1.6 INTERNAL POWER SUPPLIES

A. Electrical Design

Basic circuits were designed for the power supplies and voltage regulators.

There are five basic types of power supplies: 9, 16, 30, 60, and 120v dc; the preliminary rack locations for these are shown in Figure 6-35. All power supplies use the same circuit configuration: a 3 phase delta-Y transformer, full wave solid state bridge rectifier, and single section LC filter; each includes circuit breakers, fault indicating circuitry, and

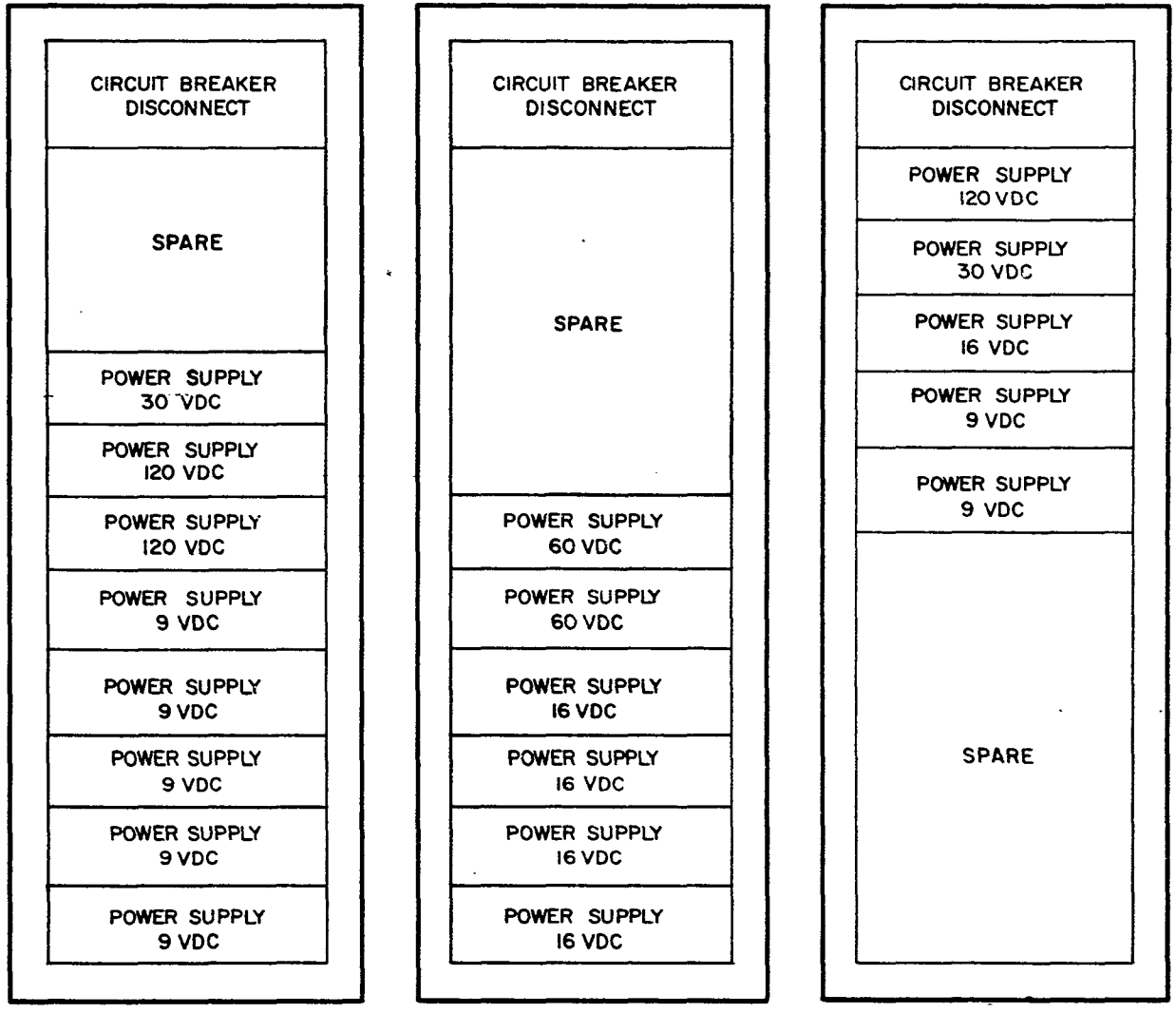

Figure 6-35 Internal power supply rack layout

front of panel indicator lamps; outputs are isolated from ground to permit either positive or negative ground.

Output voltage regulation is accomplished at the rack where the voltage is actually used, hence the regulator chassis do not show on Figure 6-35. The same basic dc regulator circuit is being used for each voltage (6, 12, 20, 50, 100v dc); the basic fixed references are zener diodes. Preliminary layouts have resulted in requirements for ten DC Regulators, each containing up to ten regulator circuits depending on the dc requirements of the particular group.

Specifications for the transformers are being prepared. Materials for breadboarding the voltage regulators have been ordered.

B. Mechanical Design

Mechanical design effort is oriented toward packaging each internal supply in a one-half drawer unit. This type of assembly, when combined physically with a mating half drawer will form an MTE standard power supply chassis.

C. Plans for the Next Quarter

Transformer specifications, electrical schematics, and parts lists for all power supplies will be completed.

Schematics and parts lists for the regulators will be completed. Each of the five required regulators will be breadboarded and tested.

Mechanical layout drawings will be completed, and detail drawings about 90% completed. Fabrication of detail parts and printed cards will start.

6.2 EQUIPMENT DEVELOPMENT: HYDRAULIC TEST UNIT

6.2.1 INTRODUCTION

The Hydraulic Test Unit consists of the following major functional assemblies:

(a) Controller and associated peripheral equipment

(b) Electronic Stimuli

(c) Electronic Measurements

(d) Internal Power Supplies

(e) Hydraulic Test Stand (HTS)

(f) Pneumatics.

The MTE Second Quarterly Interim Technical Report contained a description of the Hydraulic Test Unit (HTU) and described items (a) through (f) above. Development effort on items (a) through (d) is covered in Section 6.1 of this report. Since these items are the same whether used in the ETU or in the HTU, development progress on these items will not be repeated. This Section (6.2) deals with the development progress on those items peculiar to or associated only with the HTU.

6.2.2 CONTROLLER SIMULATOR

A subcontractor for the design and construction of the Hydraulic Test Stand has been selected and approved by the Army. The specifications for the HTS[1] were generated and completed on August 2, 1962 by RCA.

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[1] Technical Requirement, 2 August 1962, Multisystem Test Equipment Hydraulic, Pneumatic Test Stand(s).

Since the HTS will be a subcontracted item, when completed an appropriate evaluation and test must be performed to determine that all requirements of the specification are met. To accomplish this evaluation a Controller Simulator is being designed to replace the functions and interfaces associated with the Controller, Measurements, Monitor Adapter, Switching, and Control Console of the HTS.

A. Characteristics of Interfaces

The interface between the hydraulic Test Stand and the Controller Simulator will be divided in two groups:

(1) Outputs from Simulator to HTS

(2) Outputs from HTS to Controller Simulator.

Group I

From the RCA Technical Requirement, dated August 2, 1962, covering the Hydraulic Test Stand the following types of signals will be supplied by the Controller Simulator to the Hydraulic Test Stand:

(1) Two groups of 16 relays or equivalent contacts manually controlled individually or in combination. The 16 bits will represent 4 BCD characters. (The relay contacts or equivalent will be 15 volt-ampere, 250v dc maximum.)

(2) Analog voltages from 0 to 9.99 volts dc at 1 milliampere maximum. The increments of necessary steps from 0 to 9.99 volts will be controlled manually. The stability of the dc voltage will be ±0.1%. The accuracy will be established by the simulator's digital voltmeter prior to application to the HTS.

(3) Fixed reference voltage of 10 volts dc at 500 milliamperes with 0.1 percent accuracy

(4) 28 volt power supply

(5) Input power lines and monitors

(6) Selector switches, intercabling, etc.

NOTE: The primary power necessary to operate the Hydraulic Test Stand will be 208/120 volt ac, 3 phase, 400 cps, wye-connected, 4-wire supplied by the sub-contractor during the test and evaluation of the Hydraulic Test Stand.

Group 2

The following output signals will be supplied by the Hydraulic Test Stand to the Controller Simulator:

(1) DC signals representing such parameters as pressure, flow and temperature. The range of these type parameters shall be 0 to 0.999v dc, 0 to 9.999 and 99.99v dc full scale.

This set of measurements will prove that the sensors are operational, but will not prove the accuracies of flow, rates, or pressures. The vendor will demonstrate these capabilities and accuracies to RCA prior to acceptance of the Test Stand.

(2) Minimum of one set of 4 BCD words (16 bits) which will represent on-off functions as valve closures, relay closures, etc.

The signal characteristics will consist of 0 volts ±0.5 volt representing a binary "zero"; and +6 volts ±0.5 volt representing a binary "one".

(3) Malfunction indication signal - The HTS will have provisions to supply one malfunction indication line to the Controller-Simulator. The malfunction will be represented with a +6 volt dc signal.

(4) Unit under Test Code consisting of 16 lines (4 BCD) routed from the UUT adapter to the controller simulator to test the capabilities of code generation.

The signal characteristics of these 16 lines will consist of 0 volts ±0.5 volt for binary "zero" and +6 volts ±0.5 volts for binary "one".

(5) 208/120 volt ac, 3 phase, 400 cps 4 wye connected.

NOTE: The signal source impedance of the interface points must not exceed 1000 ohms.

B. Description of the Controller-Simulator

The controller simulator (see Figure 6-36) is being designed to simulate the conditions necessary for the operation of the Hydraulic Test Stand.

The vendor will supply the 120/208 volt ac, 3 phase, 400 cps power, but the controller-simulator will provide the control and metering of this power.

The necessary relay contacts or their equivalents, (toggle switches or relays) will be supplied from the controller-simulator as will two voltages: - one v dc fixed, the other variable from 0 to 9.99v dc. Both will have an accuracy of ±0.1%.

A +28 volt dc power supply will be provided as an input to the Hydraulic Test Stand in accordance with the specifications.

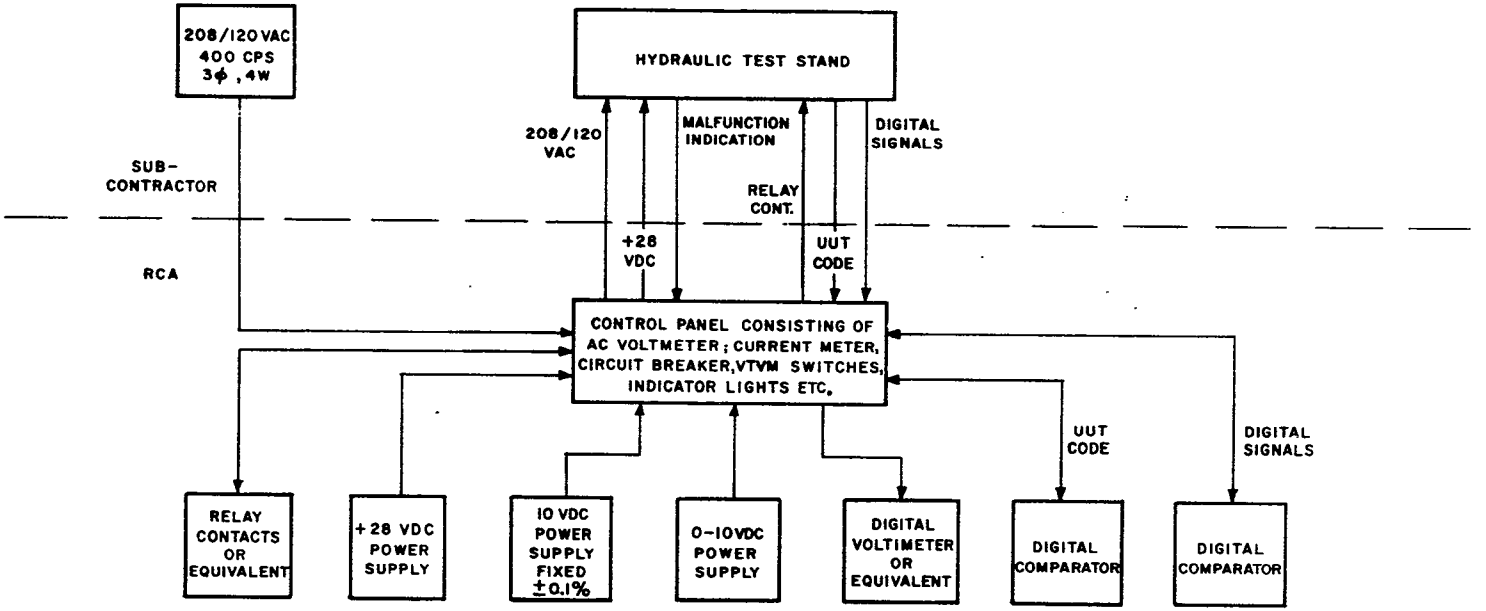

Figure 6-36. Controller-simulator block diagram

To perform the necessary dc measurements verification, the Controller Simulator will be equipped with a digital voltmeter or equivalent, having an accuracy of ±0.1%.

Additional measuring capability of the simulator will be implemented by the use of a panel mounted VTVM for noncritical voltage measurements and for malfunction indication signals.

The digital signals, UUT number codes, etc. for the HTS (which will be in BCD code) will be accepted, compared and displayed at the Controller Simulator. This particular task will be accomplished by using toggle switches and solid state comparators, drivers, relays and lights.

It should be stressed that the Controller Simulator will supply manual control only for the HTS to the simulator or vice versa. There will be no need during the HTS evaluation program for performance tests to check automation techniques.

This particular mode of operation was chosen for the basic purpose of the Controller Simulator, to supply or accept signals for the Hydraulic Test Stand evaluation of interface performance.

C. Conclusions

The above discussion and brief description of the Controller Simulator shows that with this piece of equipment considerable engineering time will be saved during the evaluation and acceptance tests of the Hydraulic Test Stand.

D. Plans

To complete the design of:

(1) the Controller Simulator control panel with all the necessary controls, switches, indicator lights, etc.

(2) the control circuits for the routing of signals between the Simulator Control Panel and the Hydraulic Test Stand

(3) the Digital Comparators and their indicator lights

(4) the indicator circuits for the HTS malfunction indication signals.

6. 2. 3 SERVOVALVE COMPONENT TESTING

A. Introductory Considerations and the Basic Problem

Implementation of a general-purpose test capability for hydraulic components within the Hydraulic Test Unit dictates the necessity of devising a singular method of testing both 3-way and 4-way hydraulic servovalves.

Valves have a high failure rate compared with other hydraulic components, since they constitute the connecting link between electronics and hydraulics in a system. Likewise, their power amplification is enormous, which means that there is a much higher probability of malfunction. Servovalve failures may equal all other electro-mechanical failures within a system.

Servovalves will be tested as components after being isolated as suspected failures by tests at systems level. To test them in their natural system environment would require a multitude of fixtures and special-purpose electronics to duplicate the actuator and closed-loop electronic circuits.

A recent trip made by RCA personnel to Redstone Arsenal, has revealed that certain types of UUT's tested and repaired in the HAWK System at third and fourth echelon are identical types found in the Mauler System, with the exception of the servovalves. Previously, a drive magnet test set was provided as HAWK test equipment for performing quiescent leakage and current unbalance tests. Subsequent maintenance allocations have been deleted. The apparent reason is the skill level required for testing and the fact that these tests singly do not constitute a sufficiently complete test.

B. MTE Hydraulic Test Set Approach

The MTE approach is to design test equipment that can not only diagnose problems encountered in rejected servovalves, but can also be used to set up disassembled valves in accordance with proper specifications.(*)

Two types of tests will be performed on all servovalves: open-loop and closed-loop. The open-loop test checks the flow versus differential current characteristics of the valve. The closed-loop test provides information on the milliampere unbalance of the servovalve, the amount of internal leakage, existence or lack of contamination in the valve, and external seepage from the valve.

C. Open-Loop Tests

The open-loop flow versus differential current test will be carried out using an RCA-developed constant current generator (see 6.2.4) capable of supplying differential current from 0 to plus or minus 25 ma into a load whose resistance value depends on the solenoids encountered in different servovalves. The desired amount of current will be obtained by automatically programming appropriate resistances into the current generator circuit.

Figure 6-37 shows the setup for open-loop testing. The flow measuring device will be a hydraulic motor. A hydraulic motor can accurately record oil flow at any temperature, and can be stalled without damage. This is essential in the closed-loop quiescent test. Use of a hydraulic motor instead of a linear actuator avoids critical time involved in

(*)Matched parts are not interchangeable, i.e., spool and sleeve assemblies must be kept together. This also applies to solenoids.

flow measurements. The motor may be run continuously in either direction. Coupled by an adapter to the servovalve, the motor can handle valves with 1/2 to 10 gpm flow at speeds up to 4,000 rpm.

A magnetic pickup tachometer measures the velocity of the hydraulic motor; the tachometer will provide a counter readout proportional to the flow through the servovalve.

Tachometer operation may be achieved for any rotating machine without mechanical coupling by converting the shaft revolution to electrical pulses.

Although many refinements are possible within a particular configuration for various applications, a basic test circuit that provides DC or pulse output proportional to the number of shaft rotations when speed is above 30 rpm is indicated in Figure 6-38.

The second peak voltage of Ti is several times greater than the operating voltage of zener diode CR1. The squared wave resulting from the clipping action of CR1 supplies a charging current to C1 through CR2, R and across M. After a time determined by the total circuit Resistance and Capacatance, C1 is 99% charged and remains so until the end of the pulse dwell time. When the pulse is returning to zero along its trailing edge, C1 discharges through CR3 and CR1, the latter having shifted to its forward conduction characteristic due to the inverse primary wave. The capacitor is now reset and ready for succeeding pulses. The metered current is proportional to the average value of the charging current and the repetition rate. This result may be calculated as

$$I_o = \left[ECR_1 - (ECR_2 + ECR_3)\right] / R \; A \; ti/T$$

where, I_o = measured current across internal resistance of metering circuit.

ECR_1 = zener diode voltage
ECR_2 = instantaneous peak voltage of CR_2
ECR_3 = instantaneous peak voltage of CR_3
R = total metering circuit resistance
A = form factor of exponential wave equal to 0.3 (assumed)
ti = changing time of C_1 equal to 4.6 RC_1 (assumed)
T = Pulse duration in seconds

The measurement of both velocity of shaft rotation and rate of bidirectional response may be performed in the utilization of this circuit for testing hydraulic servo systems. The output may be measured as a DC voltage if a configuration shown in Figure 6-38 is used at the output or it may be measured as the number of events per unit time (by means of an eput meter).

D. Closed-Loop Tests

The setup for closed-loop testing is shown in Figure 6-39.

The DC amplifier closes the servo loop and holds the system in a quiescent condition by developing differential current to compensate for mecanical and hydraulic unbalance in the servovalve. The movement of the hydraulic motor is servo-controlled and driven to zero. The electric clutch disconnects the potentiometer from the hydraulic motor in case speed exceeds the manufacturer's recommendation (Approx. 30 rpm).

From the test setup (Figure 6-39) information may be obtained on the following parameters:

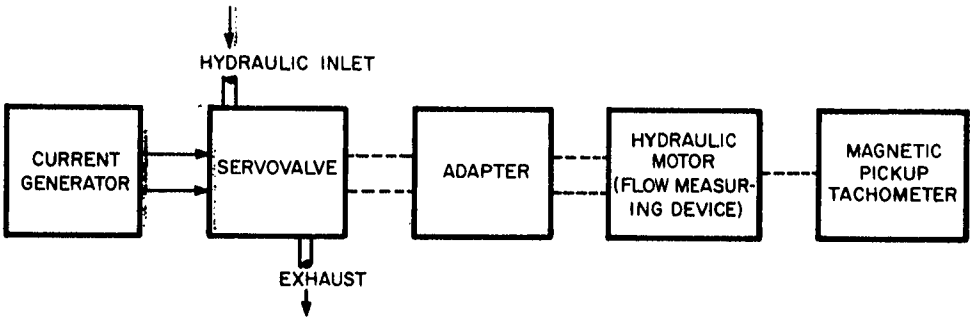

Figure 6-37. Block diagram of servovalve open-loop testing setup

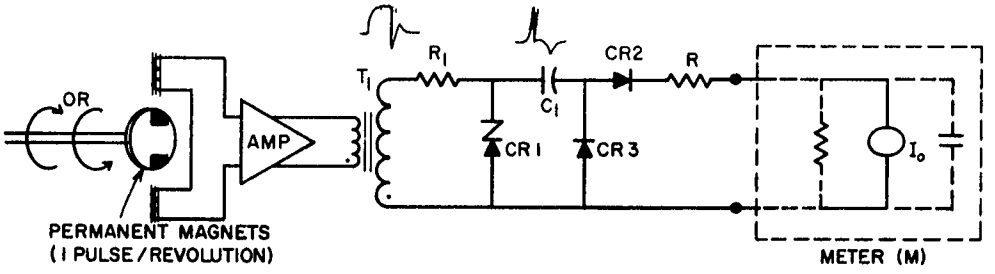

Figure 6-38. Servovalve test circuit for speeds above 30 rpm

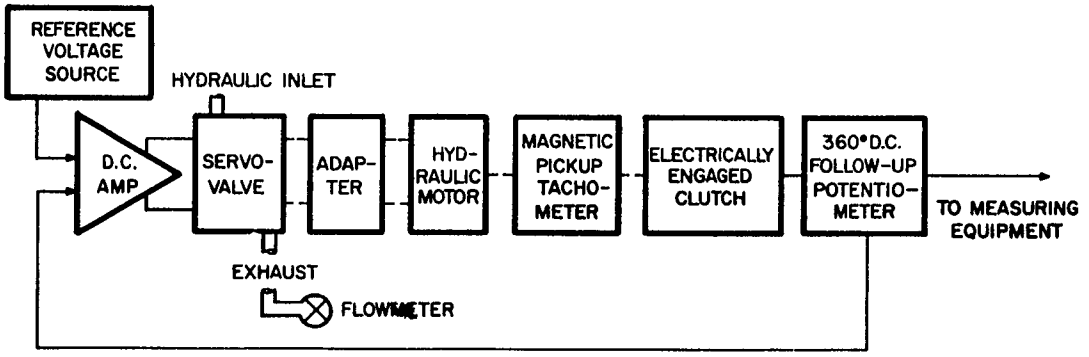

Figure 6-39. Block diagram closed-loop servovalve test setup

(1) Current unbalance-the differential current necessary to overcome any mechanical or hydraulic unbalance in the valve will be measured when the tachometer output is near zero.

(2) Internal oil leakage - the amount of oil that flows directly from pressure inlet to exhaust without doing any useful work will be measured at servovalve null by a flowmeter in the exhaust line.

(3) Valve contamination will appear as low, random frequency and amplitude oscillations at servovalve null.

(4) External seepage will be checked visually.

E. Parameters and Characteristics of Interest in Testing Servovalves

Open-loop flow gain plots are important in performance analysis because servovalves are usually designed with linear relationship between differential current and flow (see Figure 6-40) for compatibility with any linear servo system.

Since the output of the magnetic pickup tachometer is fed to a counter, the above plot would be transformed into the plot shown in Figure 6-41, where flow is represented by events per unit time (eput).

Flow will be measured at points of maximum differential current; if these points fall within specifications, flow values for less currents would be within specifications. The converse is not necessarily true, since degradation in flow-gain takes place first at the points of maximum current, as shown in Figure 6-42.

In actual test, for each value of differential current there will be a tolerance on the valve flow output. The straight line curve of Figure 6-41 will take the form of a belt of acceptable values, as shown in Figure 6-43.

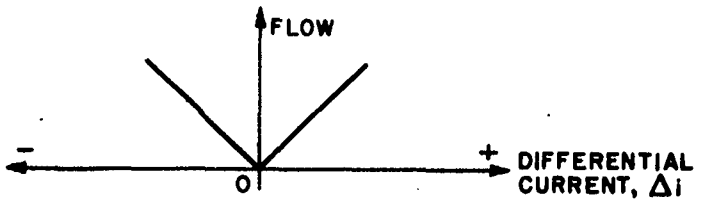

Figure 6-40. Differential current vs flow characteristics

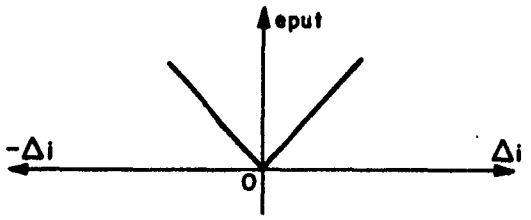

Figure 6-41. Flow representation by Events per Unit Time (eput)

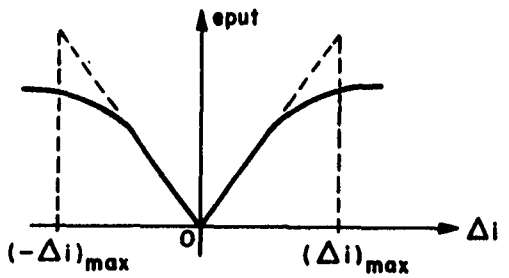

Figure 6-42. Degradation of flow-gain occurs first at points of maximum current

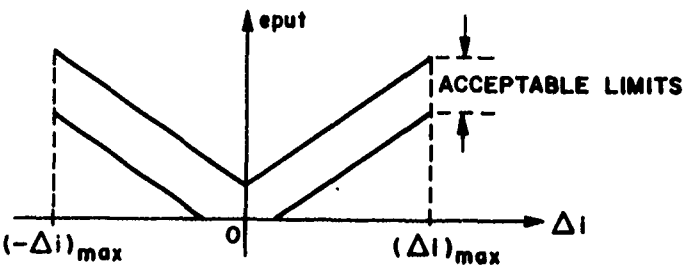

Figure 6-43. Acceptable limits of valve performance

Any error in these tests minimized by automatically programming the differential current and not relying upon operator adjustment.

Figure 6-44 shows a typical reject due to excessive valve gain. In a closed-loop subsystem test, this valve would appear unstable.

A typical reject due to low gain is shown in Figure 6-45. In a subsystem test, this would show up as poor in response but inherently stable.

A characteristic constituting rejection due to excessive current unbalance is shown in Figure 6-46.

F. Field-Adjustments Possible on Servovalves

Using test setups in Figure 6-37, 6-38 and 6-39, adjustment of servovalves may be made as follows:

(1) Armature and pole-piece gap may be mechanically varied in variable-gain valves (solenoid-operated) to bring them within specifications for current unbalance and flow gain characteristics;

(2) Maximum torque-motor travel may be adjusted and the valve nulled out if fixed-gain type (torque-motor operated).

Low frequency audio sine-wave input may be injected to provide dither frequencies for servovalves requiring a superimposed dither for normal operation. This enables the "buzzing" of a servovalve that is malfunctioning due to excessive contamination.

If servovalves are encountered with nonlinear relationships between flow and current as shown in Figure 6-47, the proposed test equipment

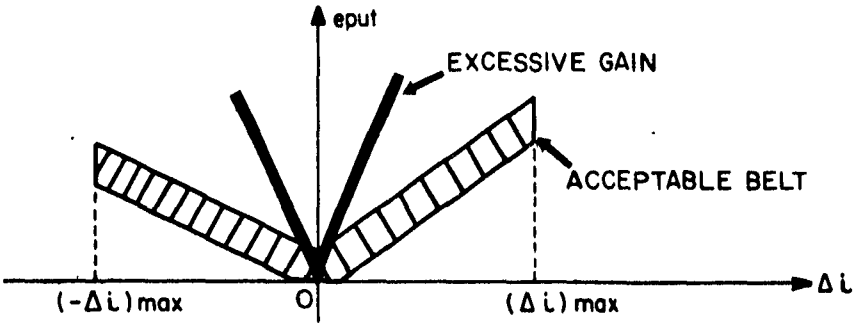

Figure 6-44. Rejection due to excessive gain

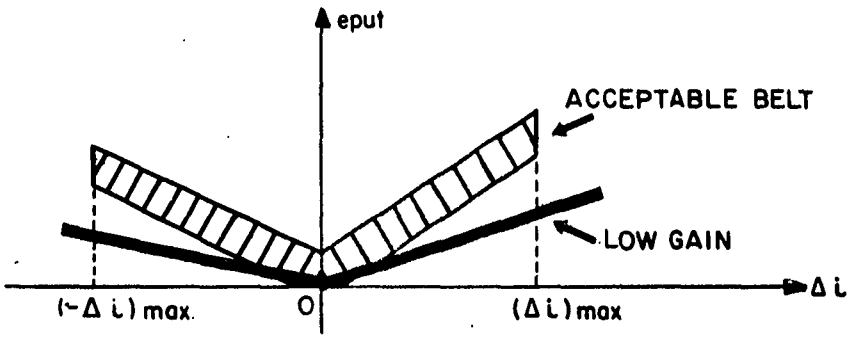

Figure 6-45. Rejection due to low gain

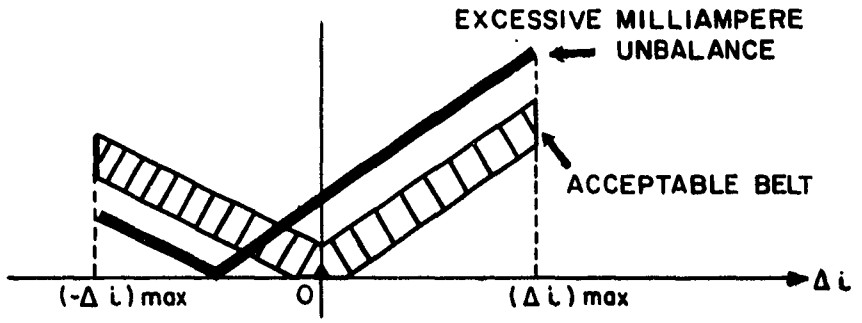

Figure 6-46. Rejection due to excessive current unbalance

would still be capable of testing them by checking several points of applied differential current, such as plus or minus 2, 4, 6, 8 ma, instead of the maximum points only.

G. Methods of Handling 3-Way Valves

The difference between 3-way and 4-way valves used in missile systems should be noted. A 4-way valve ports and vents oil simultaneously through two lines, as seen in Figure 6-48. These lines are connected to an actuator, thereby providing a controlled force to some load.

A 3-way valve ports and vents oil to the actuator through one line. The actuator is generally called a "bias actuator" with differential areas on either side of the piston.

Figure 6-49 shows the connection of the 3-way servovalve to the actuator. The task performed is similar to that shown in Figure 6-47, however, the system characteristics of the two are different.

The test setups in Figures 6-37, 6-38 and 6-39 must be modified for testing 3-way servovalves; Figure 6-50 shows a proposed configuration with a pressure biasing system.

H. Summary Evaluation of Proposed Test Setup

The system described for analyzing servovalves yields much useful diagnostic information with a small quantity of test equipment and is included as a part of the Hydraulic Test Stand Design. The entire system lends itself to the setup and adjustment of valves, if this becomes a requirement for 3rd and 4th echelon maintenance. No definite time base is required to measure flow as would be required with linear piston actuators. After the appropriate differential current has been programmed into the valve, continual mechanical adjustment may be made and instantaneous readout of flow indicated and recorded. This readout can exist as

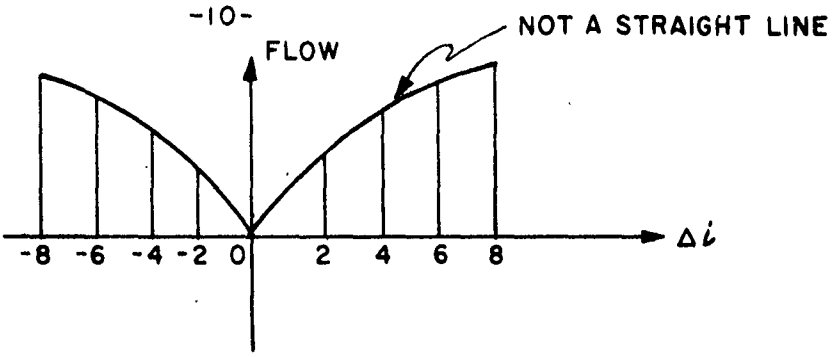

Figure 6-47. Nonlinear relationship between flow and current

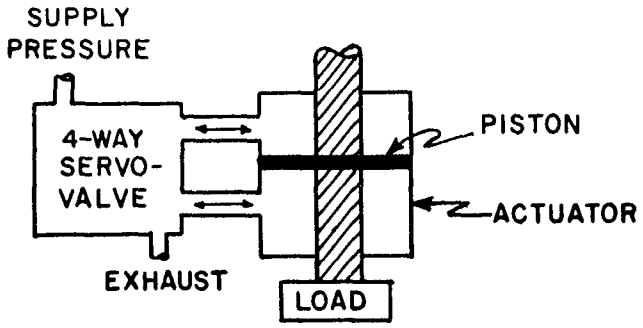

Figure 6-48. A 4-way servovalve

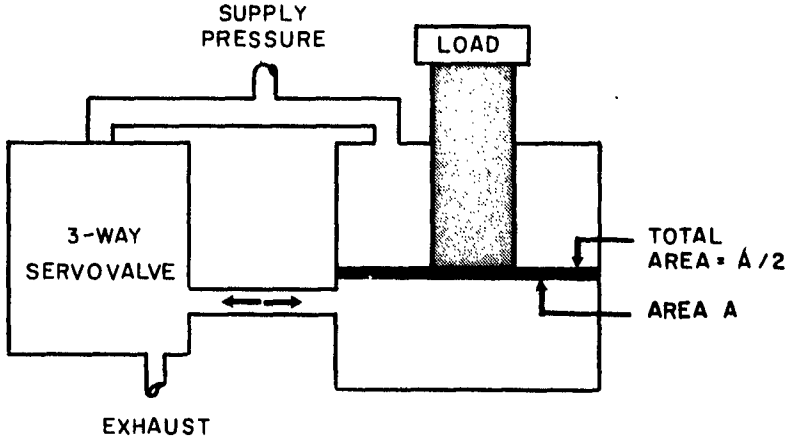

Figure 6-49. Three-way servovalve output connection

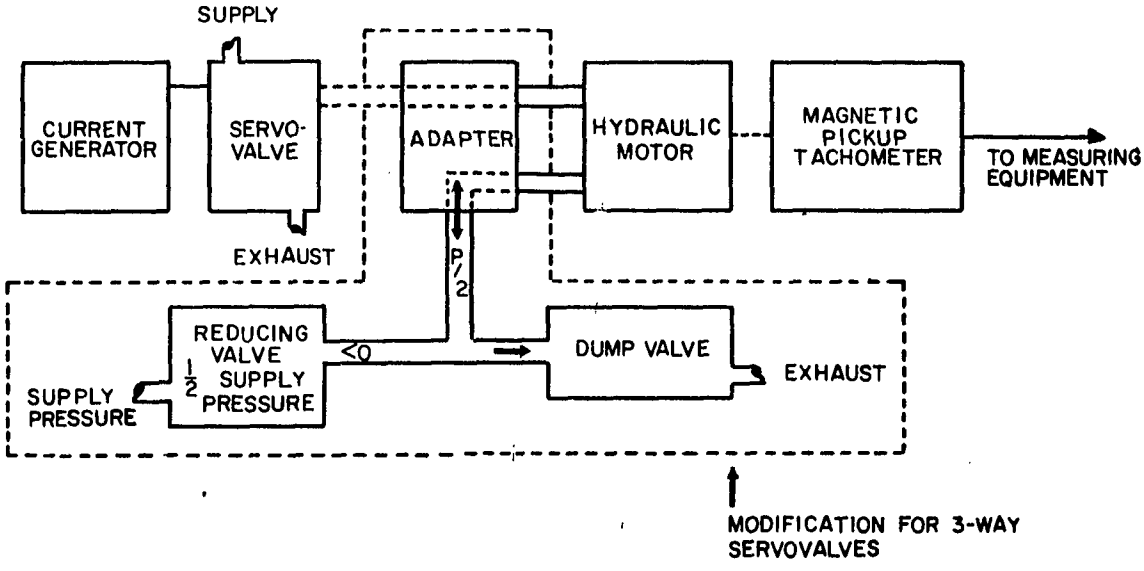

Figure 6-50. Modified servovalve testing configuration

long as the operator requires it.

6.2.4. PROGRAMMABLE CONSTANT CURRENT GENERATOR

A. Basic Approach

To ensure accurate stimulation for obtaining flow data in testing a servo-valve, a control circuit that may be programmed and that has constant current characteristics is necessary. A circuit that has proved satisfactory for dynamic current power supplies is shown in Figure 6-51.

This circuit uses the constant-current characteristics of a grounded-base transistor. The transistor chosen should have a high current gain (h_{fe}) to handle the circuit losses and expected load currents. It should also be of sufficient power rating to tolerate the power dissipation in the circuit. B_1 is a mercury battery or low-impedance Zener diode voltage source to control the base bias of the transistor, and thereby the load current. The circuit must be supplied with a well-filtered voltage source of about 40 v. Since Q_1 will not regulate or smooth out amplitude variations caused by ripple, the dc supply must have a very small ripple content.

Grounded-base current generators exhibit a 1000 to 1 effective series resistance to load regulation characteristics, which is approximately 10 times more efficient than the usual series ballast resistor used in simple current regulating circuits.

B. Existing Design of Current Generator

To achieve operating capability under extreme temperature excursions for which MTE circuitry is being designed, silicon transistors are utilized. This has altered the basic circuit somewhat ; however, the theory and practicability of design is inherently identical. The circuit

is illustrated in Figure 6-52.

By adjustment of the potentiometer (P), a discrete amount of current is produced through the load, in this case a servovalve solenoid. In a servovalve, there are tow such solenoids; simultaneous channelling of current to both coils will produce a net or differential current that will cause the servovalve to produce flow to the actuator. The usual range of supply current to most varieties of servovalves is zero to 25 ma, maximum. Usual servovalve solenoid resistances range from 500 to 3500 ohms.

Figure 6-53 shows the present version of the constant current generator, which has been breadboarded and which works as designed.

The breadboard model features single potentiometer control of differential current flow. When incorporated into the test system, the potentiometer will be replaced by a programmable set of incremental resistance that will be switched in automatically according to test directions. The scaling resistances R_x will be programmable in steps of 500 ohms from zero to 3000 ohms. They will compensate for the different solenoid resistances of servovalves (ranging from 500 to 3500 ohms) by adding or subtracting resistance in each leg of the circuit to provide a continuous load of 3500 ohms. In this manner, the circuit can be designed for a normalized load of 3500 ohms.

C. Plans for the Next Quarter

The servovalve control current generator circuit will next be tested for temperature stability; in addition, the variation of load current with power supply variation will be determined and improved, if necessary. A higher-beta transistor will be utilized for these tests which should also improve the stability and regulation characteristics.

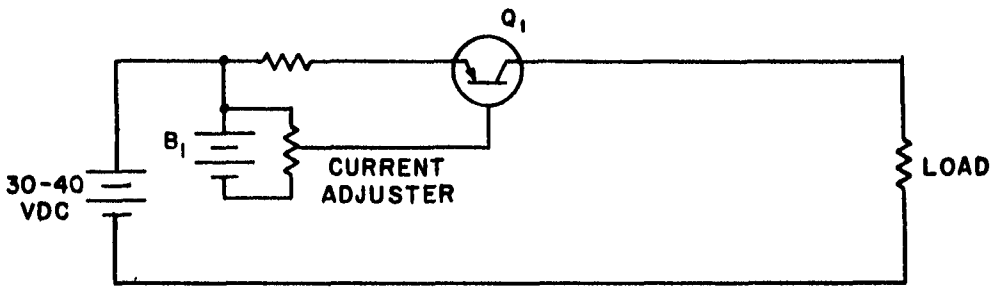

Figure 6-51. Basic constant current circuit

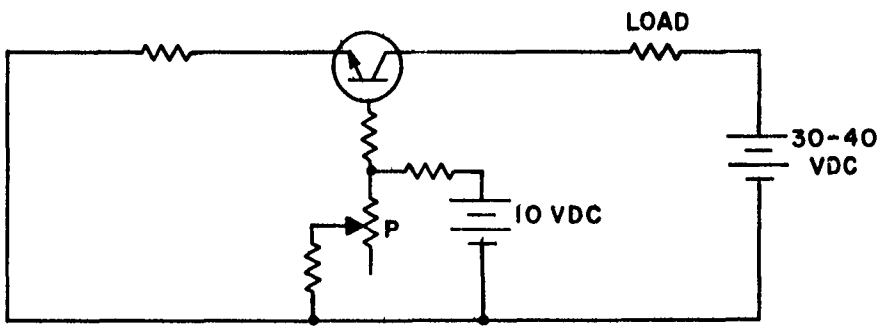

Figure 6-52. Basic constant current circuit modified for use with silicon transistors

The possibility of using a current generator having programmable Zener diodes instead of resistances, will also be investigated. This circuit is shown in Figure 6-54.

In thi particular circuit, selection of a voltage reference Zener diode, CR_1, would compensate for voltage variations and would provide tighter current control from load resistance variations. This alternate circuit would require temperature compensation by inserting a temperature-sensitive resistor with a positive temperature coefficient of resisitivity in the emitter circuits. The temperature-sensitive resistor should have sufficient power handling capability to prevent excessive self-heating. The resistance in series with the Zener diode must carry the base current and the diode current as well as limit the power consumed by the diode.

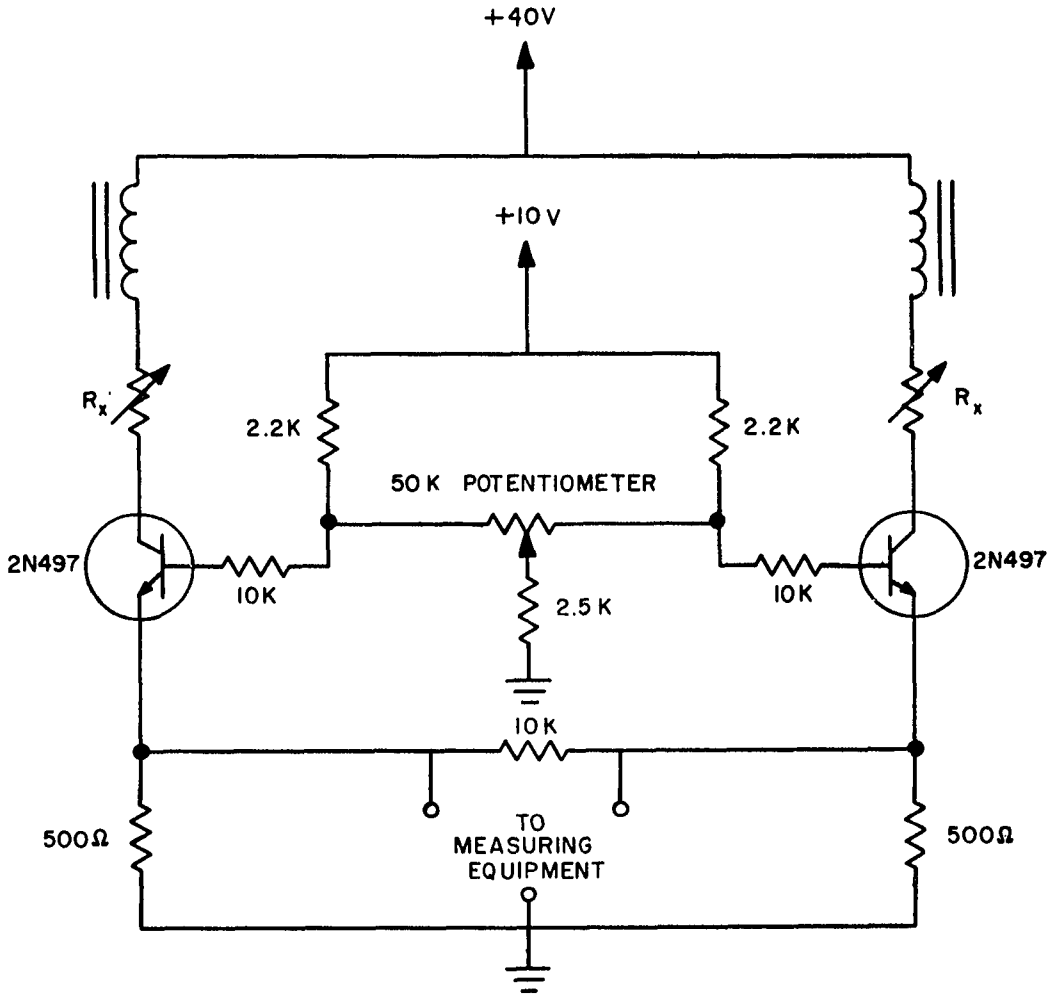

Figure 6-53. Breadboard version of constant current generator

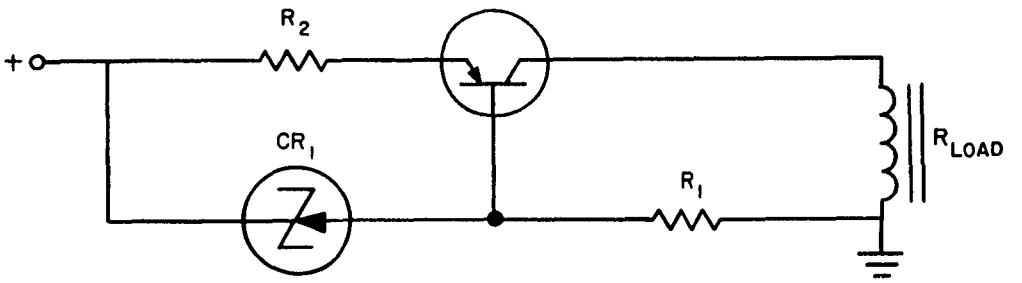

Figure 6-54. Alternate circuit configuration

SECTION 7

DETECTION AND ANALYSIS OF FLUID CONTAMINATION, FILTRATION AND CLEANING IN MTE

7.1 DETECTION AND FILTRATION OF CONTAMINATED OIL

7.1.1 INTRODUCTION

In the present concept of MTE, there is no provision for determining the contamination level of oil in either the Hydraulic Test Stand or the Mauler UUTs. This is true for other weapon systems at 3rd and 4th echelon maintenance levels. However, the MTE Hydraulic Test Stand as proposed by Greer* does include provisions for automatically monitoring pressure drop across the filter. When the filter has removed all of the contaminates that it can hold, the pressure drop becomes excessive, generally greater than 120 psi. This pressure drop closes a set of contacts causing an electrical display to indicate that the stand can no longer effectively filter oil. The filter should then be removed and replaced.

Investigations indicate that the technique for filtering oil as originally proposed by Greer will not be adequate for MTE. Low pressure filtration of oil is much more effective than filtration in a high pressure line. Since the Hydraulic Test Stand must operate with a nearly "super clean" oil** a low pressure bypass filtration system will be specified in the Hydraulic Test Stand subcontract soon to be awarded. This filtration system is shown schematically in Figure 7-1.

*Greer - Proposal Reference ESRE62-132 dated August 18, 1962.

**"Super-Clean" Oil generally regarded as a filtration level in which the particle count does not exceed 8,000 in the range of 6 to 25 microns for a 100 ml sample.

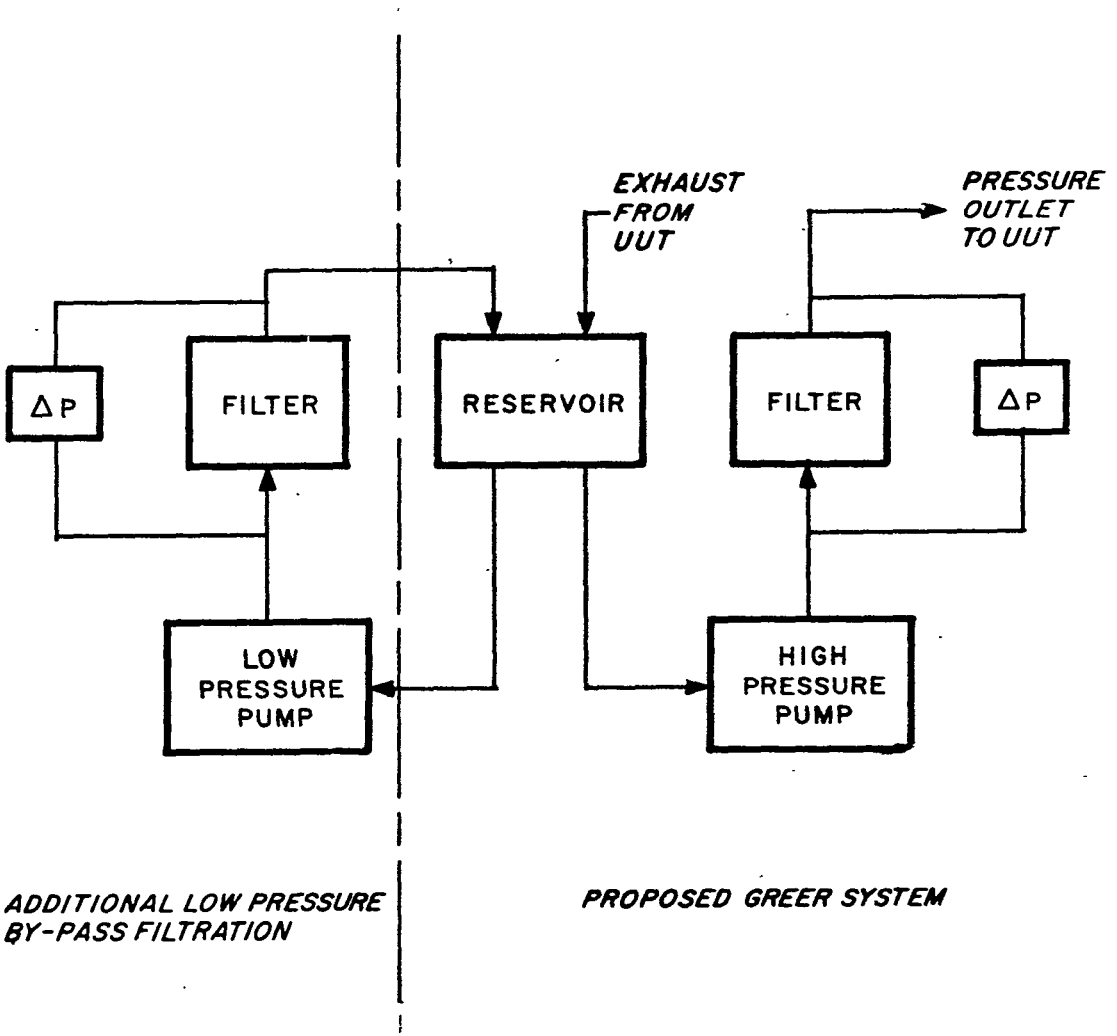

Figure 7-1. Filtration system

Provisions will be made to operate this low pressure bypass filtration system independently from the Hydraulic Test Stand. One of the work loads to be imposed upon the hydraulic stand will be flushing of contaminated servo valves; this may require the bypass system to run continuously for several days in order to reduce the contamination to an acceptable level. With the filtration set-up as shown in Figure 7-1, the hydraulic stand will be capable of self-cleaning in most operational situations that will be encountered. However, should the oil within the stand be mixed with that of a contaminated UUT, (e. g. evaluating servo hydraulic subsystems) this mixture could overload the filtration capacity of the test stand. This would require the hydraulic stand to be shut-down while the bypass filtration system cleans the oil. To assure that the oil in the hydraulic stand is kept clean at all times, a likely solution would be a portable filtration cart such as the one currently being used in the HAWK Missile System*.

7. 1. 2 CONTAMINATION DETECTION

MTE will be capable of performing servo hydraulic tests that will indicate a suspected contamination problem. Tests will be performed closed loop with the UUT in a quiescent condition. A contaminated system shows up as a low level oscillation; both the amplitude and the frequency are random. The frequency is generally below that of the system resonant frequency. In order to definitely establish that the oil is contaminated, a sample must be examined.

Contamination in a nonservo system such as the Mast Stow in the Mauler Pod would cause the system to be sluggish. Excessive contamination

*A more comprehensive description of this unit is covered later in this report.

could cause internal damage to the system, particularly to "hydraulic fits", long before external symptons were noted*.

The Mauler "on-turret" hydraulic system will undoubtedly be one of the most difficult hydraulic systems to keep clean that will be encountered in any missile or support system. There is a single 11 gallon per minute pump feeding six different hydraulic subsystems. Contamination generated in any one of the six subsystems will immediately make itself felt in the entire "on-turret" system. This situation is made worse because of the small amount of oil stored in the reservoir (approximately 2.6 gallons). If the reservoir were larger it could absorb greater amounts of contamination. Once a subsystem has a suspected contamination problem, without special equipment to analyze the exact amount of its contamination, the only alternative would be to shut the system down and spend 2 to 3 hours filtering the oil. This is very time consuming, particularly when at the end of the filtering cycle it may be determined that contamination was not the cause of a UUT malfunction. It then becomes apparent that to efficiently and expeditiously perform the analysis of the UUT problems, additional means must be provided to analyze oil contamination levels.

7.1.3 METHODS AND EQUIPMENT FOR CONTAMINATION DETECTION

The ideal solution for determining particle contamination level would be an automatic method. Some of the better known methods are described below:

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*"Hydraulic fits" - terminology used to describe a particular type of hydraulic seal normally associated with spools and sleeves. Diametrical clearances are held so close that the passage of high pressure oil is prohibited (approximately 150 millionths of an inch).

(1) Coulter Counter - Manufactured in Elmhurst, Ill. This unit measures the change in conductivity as oil passes through an orfice located between two electrical plates. This unit has not proven reliable or rugged enough for MTE.

(2) Hiac Counter - Manufactured by High Accuracy Products, Corp., Clarement, Calif. A light beam is directed through the fluid system so as to impress particle images on a photo-tube at the opposite side. Any foreign particle in this stream interrupts a portion of the light beam, causing a change in the output signal from the phototube proportional to the size of the particle. This principle would be excellent for automation. This unit has been used only in laboratory work; a redesign would be necessary for field use.

(3) Eppi Precision Products - Utilizing a light transmission technique, fluid is passed through a double filter. The upper filter removes all particles and the lower filter is discolored by any color bodies. The two filters are inserted individually between the light source and a photocell. The difference in readings between these two can be directly related to the amount of contamination present. This technique lends itself to low viscosity fluids such as jet fuel and has met with only moderate success with hydraulic oil.

(4) Millipore, Bedford, Mass. - Contamination level is established as a silting index. Oil is filtered through a membrane having a uniform pore size (0.8 micron) at a high constant pressure differential. Particles trapped in the filter cause a delay in the rate of flow. (This is expressed as a Silting Index). This technique is independent of viscosity and temperature. However, there are many drawbacks - it is delicate, difficult to calibrate, and too bulky.

(5) Thermal Control Co., Sussex, England - This technique utilizes a microscope for comparison of an oil sample (collected using a Millipore Bomb Sampling Kit) with that of a pre-established sample or samples. This method has a great deal of merit except that both specimens cannot be viewed simultaneously, resulting in some degree of error.

(6) Millipore Bomb Sampling Kit plus a microscope for determining the particle count - The bomb kit contains all of the components necessary for taking samples of oil from a pressurized system. This is accomplished as shown below in Figure 7-2.

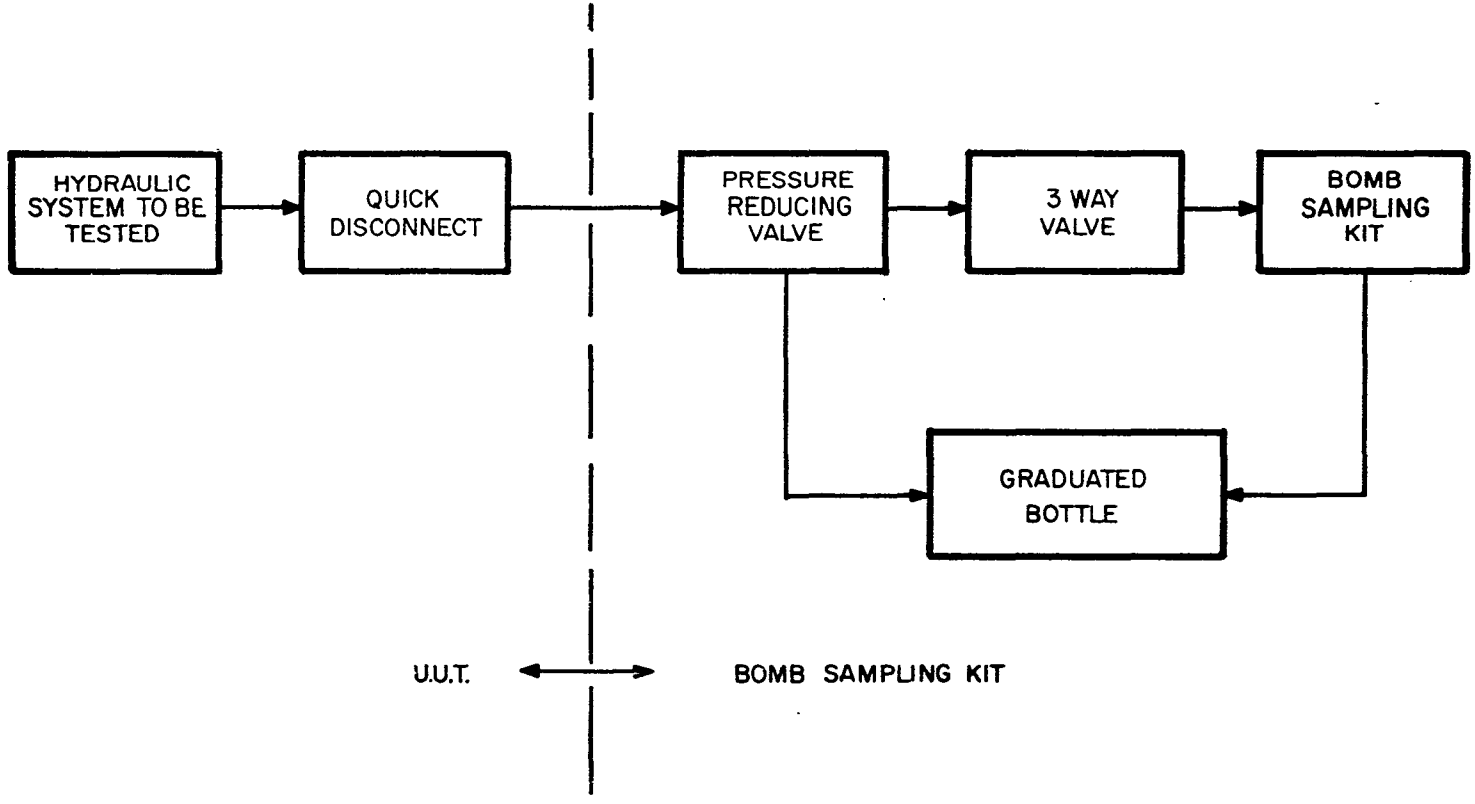


Figure 7-2. Millipore system of contamination detection

The pressure reducing valve is used only when oil is sampled in the high pressure side of the system. The three-way valve is positioned to first direct oil to the graduated bottle, bypassing the bomb sample monitor. This flushes the system up to the monitor. Next, the three way valve is positioned so that 200 cubic centimeters of oil flows through the monitor. Monitors are disposable, plastic holders with a filter disk sealed tightly between the top and bottom halves. Fluids may be passed through the monitor leaving contaminates on the filter surface. A cellulose pad is placed beneath the filter for support and to distribute fluid flow over the entire filter surface. The top half of the monitor may be removed to expose the filter paper for removal and examination.

The filter sample is placed on the microscope stage, the light intensity and position adjusted to obtain maximum particle definition, and particles counted in the 25 to 100 micron range. An exact step by step procedure titled "A Rapid Field Method for a Particle Count Analysis of Suspended Solids in Fluids from Pressurized Systems", is available from Millipore.

This technique requires some operator education and participation; however, the entire counting process may be completed in 5 to 10 minutes.

The merits are:

(a) The self-checking capabilities are excellent. Millipore has reference slides, identical in appearance to those of the Bomb Sampling Kit, that are photographic reproductions of samples with particle count accurately established. In the field the operator can use these slides to cross-check his equipment and counting techniques.

(b) Simplicity - The only equipment necessary to make the particle count is a light source and microscope. This technique is the simplest of those considered.

(c) Calibration - There is no electronic equipment to keep in calibration.

(d) Portability - This is the smallest particle counting equipment considered.

7.1.4 PORTABLE FILTRATION EQUIPMENT

Nankervis has developed one of the most reliable and effective portable filtration carts on the market; this has been proven in the HAWK missile systems. Filtration is accomplished by passing oil through a series of specially developed filters: first, a 20 micron, then a 10 micron, and finally a 1 micron. These filters and the technique developed by Nankervis has proven so successful under normal operating conditions that it can operate for 1000 hours without changing filters. In the HAWK system it has been proven that with 3 hours of filtration any of their hydraulic systems can be thoroughly cleaned. It is important that this filtration equipment be portable to service the contact team in addition to the hydraulic test stand.

The Nankervis portable cart is 26" by 35" by 43" and weighs 385 pounds. The unit sells for approximately $4700. The manufacturer will guarantee filtration within two micron absolute for the HAWK unit; newer units will filter to 1/2 micron.

7.2 ULTRASONIC CLEANING

There should be provisions within the Repair Unit to clean small hydraulic components, as the Hydraulic Test Unit has complete facilities for re-building and adjusting servohydraulic valves. A vapor degreasing unit does not lend itself well to MTE for the following reasons:

(1) It requires a low pressure supply of air (less than 60 psi) which is not available in the Repair Unit;

(2) It is too bulky for MTE

(3) It requires external ducts to remove fumes

(4) It can not achieve the degree of cleanliness that is inherent in an ultrasonic cleaner

(5) At least a 2:1 reduction in physical size may be achieved through the use of an ultrasonic cleaner over a degreasing tank.

An ultrasonic cleaner can clean electronic printed circuits as well as mechanical components. Sonic Systems Inc. of Westbury, N. Y. can furnish a cleaner complete with generator, power supply, and tank (inside dimensions 9" x 11" x 6" deep).

7.3 SOLVENT CLEANING

One of the greatest hazards in assembly or disassembly of hydraulic components in the field is the possibility of introducing dirt into the hydraulic system. In order to minimize this hazard, all exposed hydraulic interfaces should be thoroughly sprayed with a solvent. Three generally-used solvents are:

(1) Trichorethylene - An excellent solvent, extremely toxic and harmful to rubber compounds

(2) Petroleum Ether - A good solvent that will not harm rubber compounds, but is highly combustible

(3) Freon - A satisfactory solvent, harmless to rubber compounds, nontoxic and noncombustible.

Freon would be the best choice. A special so-called "precision cleaning agent", Freon is available from DuPont. Both the Freon and the container are microscopically clean. In actual application, the Freon should be dispensed from plastic squeeze bottles.

Another likely use for this Freon solvent would be to clean large components that cannot be brought into the shelter.

7.4 CONCLUSIONS

Pending approval of the RCA proposed RSU configuration, an ultrasonic cleaner and Freon cleaning agent will be included in the equipment list.

SECTION 8

PRODUCT ASSURANCE

8.1 PROGRESS

8.1.1 RELIABILITY

(1) The reliability block diagram and the logic diagram were up-dated to conform to the latest system configuration. Figures 8-1 and 8-2 show the up-dated block diagrams for the Electronic Test Unit and the Hydraulic Test Unit. The ETU block diagram was transformed into a logic diagram, Figure 8-3, having the form of a switching network. From this diagram, the following equation may be written to express the Reliability of the ETU for the testing of an electronic UUT.

$$R_{eu} = R_{eus}\, R_e\, R_{ips} \left(P_{a\bar{b}c}\, R_{lfs} + P_{\bar{a}\bar{b}\bar{e}}\, R_{dcs} + P_{\bar{a}\bar{b}\bar{e}}\, R_{hfs} + P_{ab\bar{c}}\, R_{lfs}\, R_{dcs} + P_{a\bar{b}c}\, R_{lfs}\, R_{hfs} + P_{\bar{a}bc}\, R_{dcs}\, R_{hfs} + P_{abc}\, P_{lfs}\, R_{dcs}\, R_{hfs}\right) R_{ma} \left[P_{d\bar{e}}\, R_{ad} \left(P_{f\bar{g}}\, R_{ac} + P_{\bar{f}g}\, R_{ra} + P_{fg}\, R_{ac}\, R_{ra}\right) + P_{\bar{d}c}\, R_{ti} + P_{de}\, R_{ti}\, R_{ad} \left(P_{f\bar{g}}\, R_{ac} + P_{\bar{f}g}\, R_{ra} + P_{fg}\, R_{ac}\, R_{ra}\right)\right] R_{dob}$$

Where:

R_{eu} = Electronic Unit Reliability

R_{eus} = Electronic Shelter Reliability

R_c = Computer/Controller Reliability

R_{ips} = Int. Power Supply Reliability

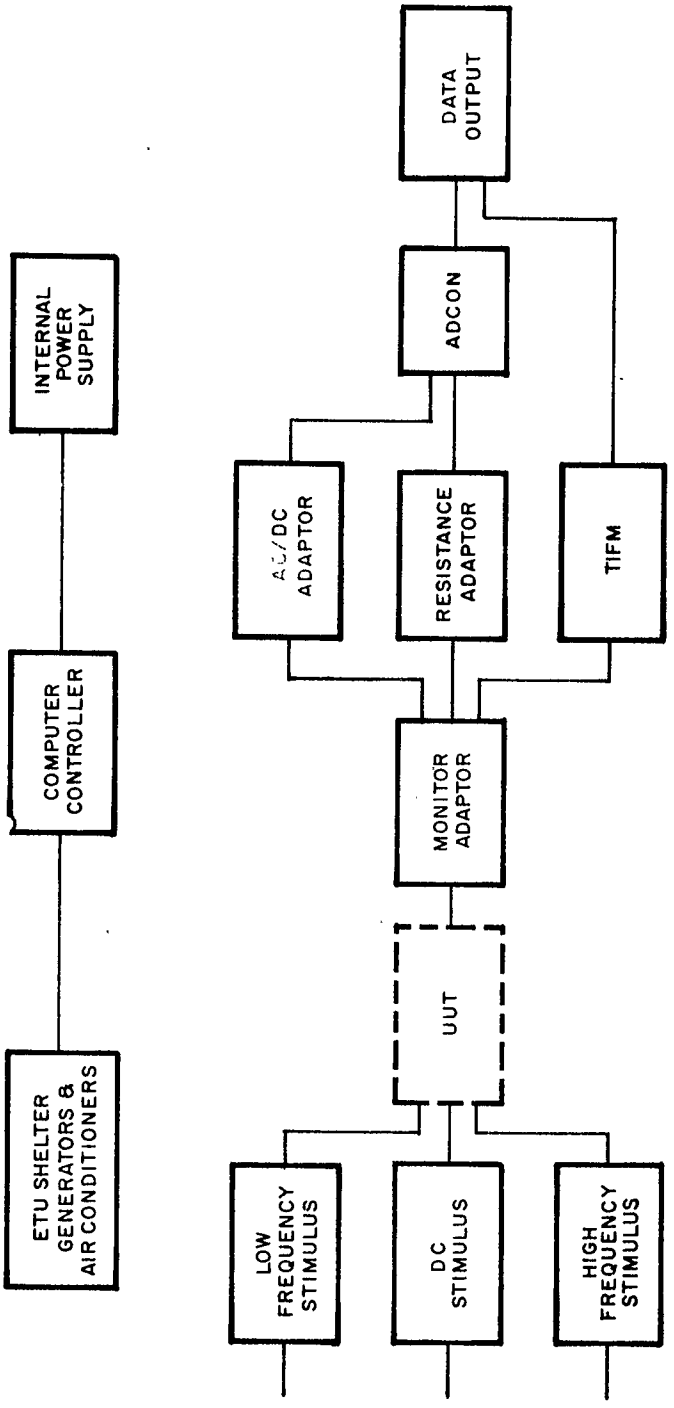


Figure 8-1. ETU block diagram

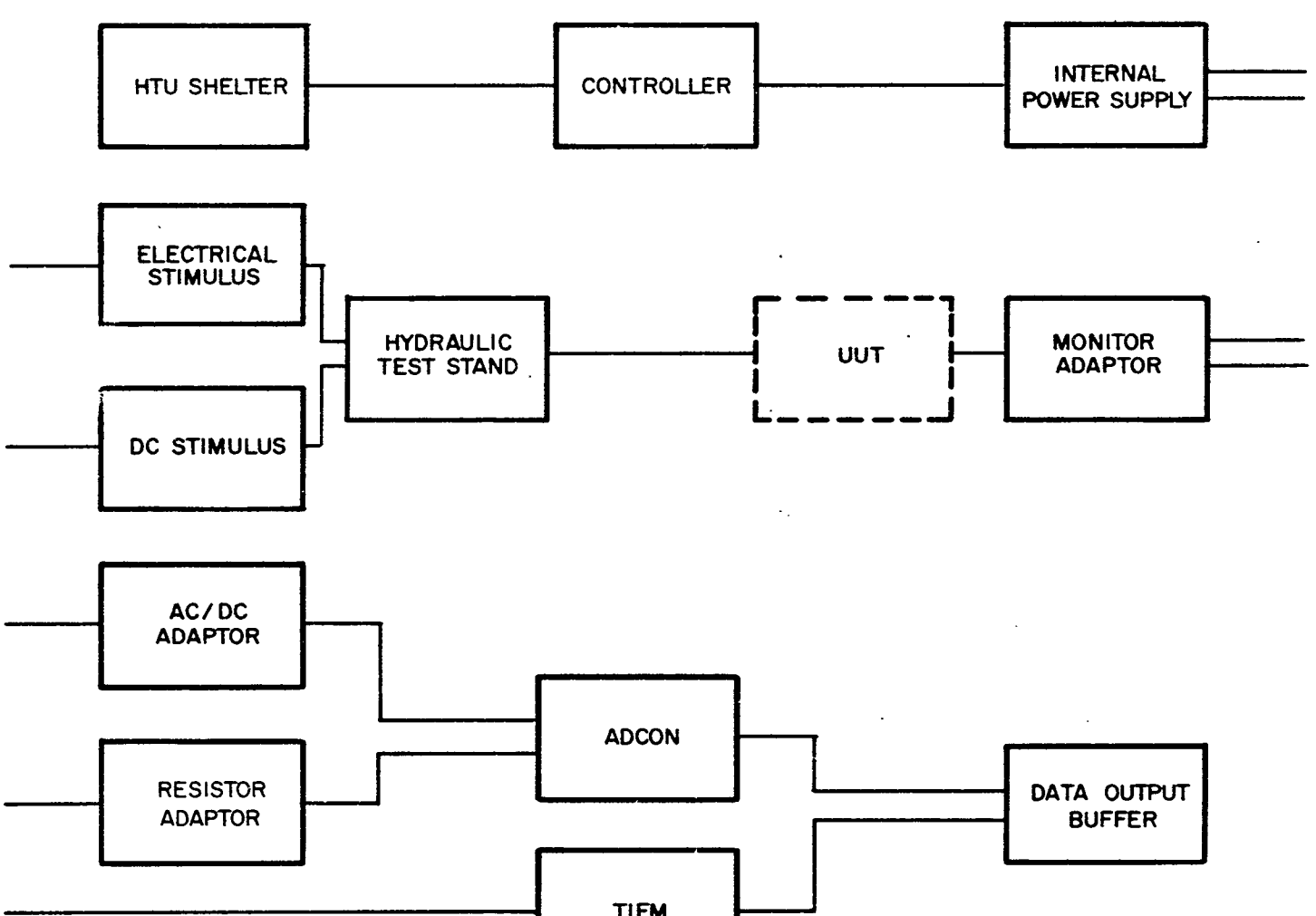


Figure 8-2. HTU block diagram

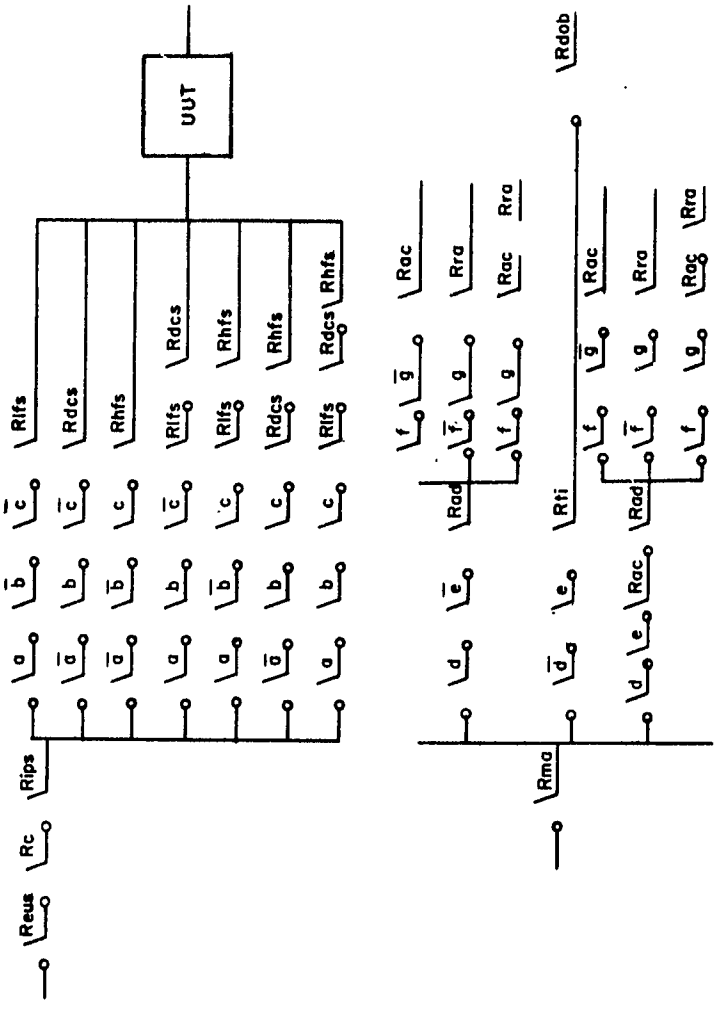


Figure 8-3. ETU switching logic diagram

R_{lfs} = Low Frequency Stimulus Reliability

R_{dcs} = DC Stimulus Reliability

R_{hfs} = High Frequency Stimulus Reliability

R_{ma} = Monitor Adaptor Reliability

R_{ad} = Analog-digited Converter Reliability

R_{ac} = AC/DC Adaptor Reliability

R_{ra} = Resistance Adaptor Reliability

R_{ti} = Time Interval Frequency Meter Reliability

P = Probability of Use

Subscripts

a = Low frequency stimulus use (a not used)

b = DC stimulus use

c = High frequency stimulus use

d = Analog to digital converter use

e = Time interval frequency meter use

f = AC/DC adaptor use

g = Resistance adaptor use

(2) Work has started on apportioning the system MTTF goal to the subsystem based on the latest design configurations

(3) The second MTTF prediction based on a preliminary parts list is being revised.

8.1.2 MAINTAINABILITY

(1) Based on the preliminary design data a preliminary maintainability prediction of the Electronic Test Unit is being calculated. The "Maintainability Check List" as presented in Appendix "C" of the Product Assurance Program Plan CR-62-547-9

is being used as a means of establishing criteria

(2) Maintainability Design Guidelines were reviewed and updated to conform to the latest design package. The Guidelines consist of a list of questions pertinent to equipment design incorporating the following general areas:

(a) Internal and external accessibility
(b) Packaging
(c) Displays--visual and audible
(d) Controls--adjustments
(e) Test points--availability and identification
(f) Labeling
(g) Adjustments--alignment and calibration
(h) Test equipment--tools and instrumentation
(i) Safety--personnel and equipment

8.1.3 STANDARDIZATION

The strengths and weaknesses of both silicon and germanium power transistors were studied to determine which type should be used in the MTE system. Also, a survey of RL type resistors was conducted in order to determine if these resistors can replace the RN type resistors incorporated in the millimods.

A. Silicon versus Germanium Transistors

Silicon rather than germanium power transistors have been selected for use in the MTE system based on the following considerations:

(1) The improvement of manufacturing processes for silicon material

(2) The performance of silicon transistors at high temperature environments is superior to that of germanium transistors

(3) Silicon transistors have been approved for military use and are acceptable for the 50G shock and 30G, 2000 cps vibrational requirements.

B. RL Type Resistors

RL type resistors were evaluated for use in the MTE system as a replacement for the RN type resistors in the millimods. The RL type resistors have been recommended for the following reasons:

(1) The RL type resistors have demonstrated a failure rate of 0.004%/1000 hours (Corning Glass data, 60% confidence level) as opposed to the RN failure rate of 0.025%/1000 hours. (RCA Defense Standards Volume 14)

(2) The RL type resistors are available in large quantities at a lower price

(3) The RL type resistors meet MIL-R-22684 requirements and have the same case size as the RN type resistors.

8.1.4 SAFETY

Safety parameters were included in the MTE Plan of Approach, Task and Skill Analysis, Training Aids Feasibility and New Equipment Training Report No. CR-62-547-22.

Safety Design Guidelines were prepared and included as part of the Maintainability Design Guidelines.

The Safety Characteristics Study for the MTE system has been completed in Volume 2 MTE Characteristics Study Report No. CR-62-547-29. This study included the identification of equipment and personal safety aspects.

8.1.5 VALUE ENGINEERING

(1) System and subsystem functional chart development has been started in this reporting period

(2) Training material for the management personnel has been developed and is being finalized. Initial management orientation to take place in the first quarter of 1963

(3) Specific task efforts have been undertaken on the building block and rack configuration to improve cost, reliability, maintainability and human factors

(4) Revisions and additions to the Value Engineering Manual are now underway.

8.2 PLANS

8.2.1 RELIABILITY

(1) The apportionment of the system MTTF goals to the subsystem will be completed. These assigned goals will appear in the design specifications

(2) The MTTF prediction will be updated based on the latest design configurations

(3) An orientation and training program will be prepared for use with major subcontractors.

8.2.2 MAINTAINABILITY

(1) An orientation and training program will be prepared for use with major subcontractors

(2) The preliminary maintainability predictions will be updated as design changes occur.

8.2.3 STANDARDIZATION

(1) Up-dating of the MTE Standards Manual will continue

(2) Subcontractor use of the MTE Standards Manuals will be coordinated and monitored.

8.2.4 SAFETY

(1) The Safety Program Plan will be revised to reflect the realigned safety task effort

(2) The lates system configurations will be reviewed for potential safety problems.

8.2.5 VALUE ENGINEERING

(1) Conduct sessions of the value training program

(2) Continue the development of functional charts

(3) Continue special task efforts for analysis of materials and major assemblies

(4) Complete Value Engineering Manuals revisions

(5) Participate in design reviews.

APPENDIX A

COMPUTER/CONTROLLER GROUP

A.1 GENERAL

A block diagram of the MTE Computer/Controller Group is shown in Figure A-1 The memory and program control, enclosed in dotted lines, is composed of a High-Speed Memory, Control Unit, Input/Output Buffer, Printer and Punch Control, Control Director and a Time Delay Unit. The measurement selection and stimuli control is performed by a Switching Control Buffer. The displays and controls are composed of the Visual Instructor, Control Panel, Maintenance Panel, Manual Input, test results, and Printer. Each of these functional elements (building blocks) is described later in this report.

The computer/controller consists of an RCA 3100 General-Purpose Digital Computer modified to meet the functional and environmental requirements of MTE. It is composed of a High-Speed Memory, Control Unit, Arithmetic Unit, and Input/Output Buffer; various input/output devices, displays, and controls; and a simple sequential controller (composed of a Control Director, Switching Control Buffer, and a Time Delay Unit).

In addition to being designed to perform the functions of automatic control and data processing, this computer/controller design reflects the RCA building block concept. Each element of Figure A-1 is a functional building block. That is, these blocks may be rearranged (without requiring any design changes), to form other systems of varying complexity and capability.

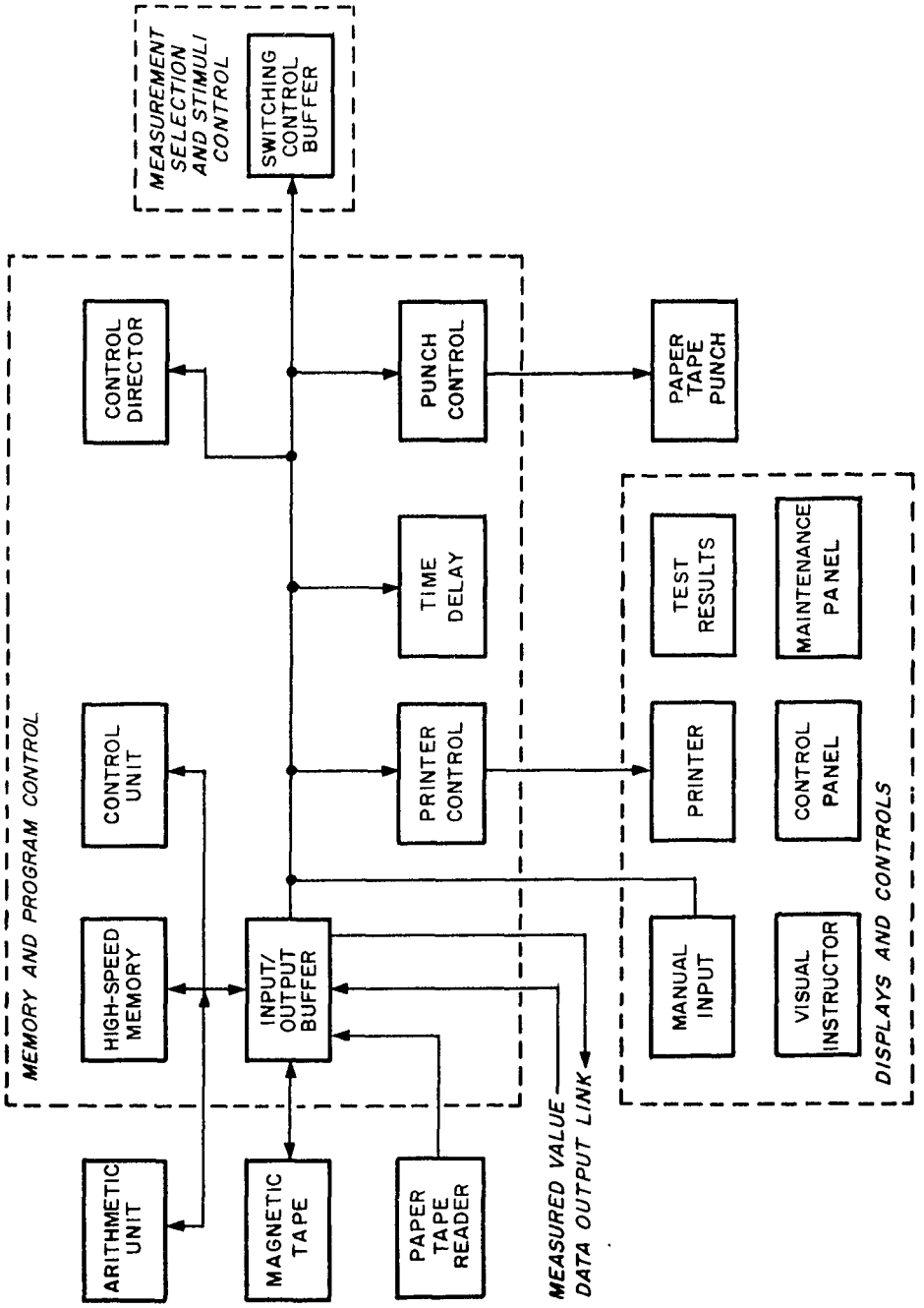


Figure A-1 MTE computer/controller block diagram

A.2 OPERATIONAL DESCRIPTION

The RCA Computer/Controller provides the computational requirements of the test procedures and the programmed control for all the stimulus and measurement groups in the MTE System. Control of the overall operation of the Computer/Controller is achieved through the execution of test sequences stored in the magnetic tape transport.

Before actual computer operation, programs consisting of instructions, data, and arithmetic constants are transferred to the memory from magnetic tape via the input/output buffer.

During performance of the test program, the control unit of the computer obtains instructions from the memory, interprets them, and issues appropriate commands to the arithmetic unit and input/output buffer.

The control director of the controller receives data from the computer via the Input/Output Buffer. It interprets these instructions contained within the data and issues appropriate commands to other units. These instructions may be commands which: (1) select particular stimuli, (2) select desired measurement test points, or (3) select the desired measurement range and function. In addition, the instructions may contain time delay or print commands.

A.2.1 FUNCTIONAL UNITS

The functions of each of the units of the Computer/Controller are described in the following paragraphs.

A. High-Speed Memory

The Computer/Controller uses as its high speed storage unit, a random-access, coincident-current, expandable, magnetic-core memory. It

has 4096 addressable word locations. The cores utilized in this memory are the wide temperature range RCA Type 233 M1 developed specifically for military applications.

A word contained in the memory consists of 24 bits plus one parity bit. It may be either an instruction or a data word. An instruction word contains an operation code, a set of index register indicators, and an address. The address part is used to denote the location in the memory which is to be subjected to some arithmetic or logical operation. The operation code is used to specify the instruction to be performed, and the index register indicators select one of three index registers. In the instruction word format the most significant six bits contain the operation code; the next three bits select the index registers; there are three spare bits; and the remaining 12 bits are the address.

Although the programmer has freedom to adopt many conventions in his choice of number systems, the usual interpretation of numbers within the MTE computer is that all numbers lie within the range $+1 \geq x \geq -1$. Under this convention the most significant bit is regarded as the sign bit; the machine point comes after the sign bit, and the remaining 23 bits indicate the magnitude. A zero in the sign bit means the number is negative. A negative number is represented in two's complement form. This convention results in an unambiguous zero.

A memory cycle time is 12 microseconds; it takes 12 microseconds: (1) to address a particular memory location, (2) to strobe the memory, (3) to read the memory, and (4) to regenerate the memory word.

This process is accomplished under control of the memory timing section. Memory input/output operations are accomplished via a 24-stage parallel memory register. Input/output rates up to 83,333 words per second are possible.

B. Arithmetic Unit

The arithmetic unit consists of an accumulator, multiplier-quotient registers, adder logic, carry logic, and an overflow register. With these functions the computer can perform three basic arithmetic operations: (1) add the contents of a specified memory location to the contents of the accumulator, (2) complement the contents of the accumulator, and (3) shift the contents of the accumulator and the quotient register (Q) right or left. All other arithmetic and logical functions are built on the framework of these three elementary capabilities. Subtraction of the memory contents from the accumulator is accomplished by complementing the accumulator, adding the memory register contents, and complementing the result. For multiplication, the multiplier is placed in the Q register and the multiplicand in the M register. The instruction is implemented by a repeated cycle in which the multiplicand is added to the accumulator contents to form a partial product which is then shifted to the right. A double-length product is formed in the accumulator and Q registers. In division, the divisor contained in the memory register is subtracted repeatedly from the double length dividend or remainder in the accumulator and Q registers, the remainder being shifted left after each step. The quotient is formed in the Q register. The number of status level changes that occur in the multiplication and division instructions and in the "shift" instructions is controlled by a four-stage loop counter.

C. Control Unit

The Control Unit consists of an operations register, time-pulse generator, and the command and status level generators. These functions store and interpret the instructions of the computer and direct the sequence of operations of the computer.

When an instruction word is read from memory it is temporarily stored in a memory output register. Interpretation of the instruction contained in the memory register is started by transferring the operation code contained in the six most significant stages of the memory register to the six-stage operation (0) register.

Outputs from the operation (0) register are combined with outputs from the timing generator to control selected stages of the status level generator. The contents of this register delineate major subdivision of the instruction or status level.

The content of the operation (0) register also is decoded by the operation decoder. Outputs from the decoder, combined with those from the time-pulse generator and the status-level generator, operate logic in the command generator to energize the command lines in an ordered sequence required for the implementation of a particular instruction.

Each required command exists for a basic time of 0.5 microseconds (determined by the time pulse generator) and effects one elementary transfer or arithmetic operation. For example, one command transfers the contents of the lower accumulator to the upper Q register; and another transfers to the operation register from the most significant stages of the memory register.

When all the commands for a particular instruction have been generated, the command generator provides a pulse to the memory timing to initiate the read-out process for the next instruction word.

D. Input/Output Buffer

The input/output buffer contains the interface circuitry between the computer and the various input/output devices. It is essentially a

language translator but also provides time buffering. This unit assembles computer words from the various single character inputs to the computer and disassembles computer words for writing out on various single character buses.

Inputs and outputs can be handled as though they were addressable memory locations. Outputs can be sent from the computer by use of a Store instruction together with an output addres.. Inputs can be brought into the accumulator by a Clear and Add, Add, or Subtract instruction, using an input address. Supplementing this scheme is a group of instructions that refer to particular pieces of in/out equipment. The Read Magnetic Tape instruction, for example, addresses the magnetic tape unit via the input/output buffer.

The input/output buffer can accept information in any of three modes: (1) octal, (2) hexadecimal and (3) alpha-numeric . Inputs from magnetic tape will be accepted in alpha-numeric mode. If the input device is the paper tape readcr, all three modes are possible.

In the octal mode, each character is converted to an octal number by inserting the 3 least significant bits of the character into the last 3 stages of a 24-bit register; the remaining bits of the character are not used. After each octal number is inserted, the information in this register is shifted three places. The process continues for each character until the register is loaded. The eight-character octal word in the register is then stored in the memory location specified by the program counter and the program counter is advanced by one count. The tape characters continue to be processed into the register and when again loaded with eight octal characters, stored into the next memory location. This process continues until a stop character is recognized.

In the hexadecimal mode, essentially the same process takes place as in the octal mode except that the input character is converted to a four bit hexadecimal code. In this mode the four least significant bits of the character are inserted into the last 4 stages of the register; the remaining character bits are not used. After each character is inserted, the information in the register is shifted four places. This process continues until the register is loaded. The six character hexadecimal word in the register is then stored in a memory location specified by the program counter and the program counter advanced by one count. This process continues until a stop character is recognized.

In the alpha-numeric mode, the last six stages of the input characters are placed into the six least significant bits of the register and shifted six places. This process continues until a four-character word is formed in the register. This word is then stored into the memory location specified by the program counter and the program counter advanced by one count. This process continues until a stop character is recognized.

The rate at which computer words are assembled is dependent upon the input mode selected and the speed of the input device. Using a given input device the rate of the octal mode load is half the rate of the alpha-numeric mode load since eight characters are required per word for the octal mode and only four characters per word for the alpha-numeric mode.

The computer is also capable of providing outputs to peripheral devices. When operating under a "Write" instruction, the input/output buffer converts computer data words to alpha-numeric characters and sends these characters to the addressed device by the data bus.

Another output mode is available in the computer. A "Store" instruction using special address locations is available for transferring the contents of the arithmetic unit accumulator to 24 discrete parallel output lines. The maximum output rate for this mode is 20,833 computer words per second.

E. Magnetic Tape

The magnetic tape unit is controlled by the computer, via the input/output buffer, by the use of Read and Write instructions under control of the program. The tape unit is automatically controlled and searched for the desired test program upon selection by the operator.

When reading magnetic tape, the Read instruction includes the memory location for loading the first word and the number of words to be loaded into the memory. Sequential memory addresses are used for each subsequent word until the instruction execution is terminated by sensing that the specified number of words have been stored. The data from the magnetic tape unit will be scanned for odd parity; a parity error terminates the tape reading process and a halt-computer/controller command is generated. Prior to executing the Read instruction, the tape is searched for the desired block of data whose address has been previously specified.

When writing on magnetic tape, the computer automatically supplies four 6-bit characters for each character to the tape unit for each output memory word. Control of character spacing on the tape is a function of the computer internal timing.

In both reading and writing operations the input/output buffer performs the functions of composing computer words from characters and of extracting 6-bit characters from computer words.

F. Paper Tape Reader

The Paper Tape reader sequences blocks of information into the computer. A "Read Paper Tape" instruction automatically provides a start command to the reader. The first paper tape character sets up the mode decoder to select one of three input modes: octal, hexadecimal or alpha-numeric. The input/output buffer then proceeds to assemble a 24-bit word from the input characters as directed by the mode decoder. For an octal input, eight 3-bit units are packed into the 24-bit memory word; for hexadecimal, six 4-bit characters are packed into the 24-bit memory word; and for the alpha-numeric mode, four 6-bit characters are packed into the 24-bit word. In the event that a parity error is sensed, a parity error display on the operator's console will illuminate; the computer will halt without storing the word with incorrect parity. The reading process continues under control of a previously loaded word counter.

Tape reader operation is described under "The Modes of Operation" section, which follows.

G. Punch Control and Paper Tape Punch

As an output device, the paper tape punch punches tapes from information stored in the memory, starting with the location specified in the address part of a Punch instruction and continuing under control of the word counter, loaded by this instruction. The computer will automatically control the mode of punching, i.e., the selection of Fieldata or teletype format. The paper tape punch will then receive a full character from the input/output buffer.

The punch may also be controlled from the control console. In this mode the punch punches Fieldata characters inserted by the operator.

H. Control Directer

The control director controls the operations of the printer, time delay, switching control buffer, and other automatic test functions. The control director recieves data serial by character from the computer via the input/output buffer under a "Write" instruction. It interprets the instructions contained within the data and issues appropriate commands to other units. The control director performs these functions by generating the timing pulses and status levels necessary to store and decode the instructions contained in the data from the input/output buffer, and those timing pulses and status levels required to carry out the operations described by the instructions.

The control director may also receive data from the manual input, as well as from the input/output buffer. The operations of the control director, in this mode, are the same as when data is received from the computer via the input/output buffer.

I. Printer Control and Printer

The printer control and printer operate under the direction of the control director. The printer control is addressed by the control director when a Print instruction is programmed in the data from the computer. The print format is under the control of the output Fieldata characters, (following the Print instruction) that are sent to the printer. Synchronizing pulses between the printer, control director, and the computer are provided.

J. Time Delay

The Time Delay unit operates under the direction of the control director. It can be programmed to interrupt the computer/controller operation for one microsecond to 166 minutes, or it can be programmed to measure elapsed time in that range while other operations are being performed.

The Time Delay unit can be utilized to synchronize the automatic test system operation with that of a unit under test, by programming the start of a delay to be controlled by the unit under test and by allowing the unit under test to control the magnitude of the time increments. When the delay is started by the unit under test, a measurement of the selected unit under test parameter is automatically made when the delay is completed.

K. Switching Control Buffer

The Switching Control Buffer provides the temporary storage and decoding of the switching words which specify the selection and ranging of all stimuli and measurement devices. The signal routing and test point selection are also controlled by unique switching words. The switching control buffer is addressed by the control director when a Switching Follows instruction is programmed in the data received from the computer via the input/output buffer. Each switching word (composed of a variable number of characters) following the Switching Follows instruction, is temporarily stored in the Switching Control Buffer until its specified control operations are performed.

L. Controls and Displays

Facilities will be provided that the operator and/or maintenance technician may meaningfully communicate with the computer/controller. Some of the facilities provided will be used mainly for computer check-out and maintenance rather than operation; the most desirable layout for these facilities has been determined by human engineering.

The maintenance philosophy for automatic test systems is that displays will be provided on the control console which will indicate which major unit is malfunctioning. Displays will also be provided on each unit to indicate the status of major functions contained therein. Therefore,

the operator's control console will contain only those displays required for normal operation and those which indicate the status of the major units.

The following controls and displays are located on the control console:

a. Visual Instructor

The visual instructor is a microfilm reader which is used to display schematic diagrams, component layouts, unit under test hookup connections, and special pictorial repair instructions.

b. Control Panel

The control panel contains the controls which require operator participation during this testing of a unit under test and the displays which inform the operator of the status of the testing routine. Where indicated, the functions listed below are both controls and displays which give positive indication of the selected control and status.

1. Unit Under Test Serial Number - Four rotary "digi" type switches select the serial number (0000 to 9999) of a particular type of unit under test. (Control and display)

2. Serial Number Acknowledge Pushbutton - Informs the test system that the operator has selected a serial number.

3. Automatic Test Pushbutton - Selects the automatic test mode of operation and starts the test system operations of the functions of this mode. This pushbutton removes any previously selected mode or submode of operation. (Control and Display)

4. Data Repository Pushbutton - Selects the data repository mode of operation and starts the test system operations of the functions of

this mode. This pushbutton removes any previously selected mode or submode of operation.

5. Standby Pushbutton - Stops the test system operation, removes any previously selected mode, and resets the complete test system to initial conditions. (Control and display)

6. Program Interrupt Pushbutton - Interrupts the test system operation at the completion of the existing instruction. (Control and Display)

7. Proceed Pushbutton - Initiates program continuation from the point at which the test system operation had been previously interrupted.

8. Print All/Print NO-GO Only Pushbutton Switch - Selects whether each measurement result will be printed or whether only the NO-GO measurement results will be printed. (Control and Display)

9. Continuous Conversion Pushbutton - Interrupts the test system operation each time that an Evaluate instruction is recognized and causes repeated measurements of the selected parameter. (Control and Display)

10. Reset Pushbutton - Resets all of the computer/control circuits to their initial condition.

11. Switching Reset Pushbutton - Allows the operator to reset all switching previously set up for the stimulus and measuring devices.

12. Remote-Local Control Pushbutton - Selects whether this control panel or a remote control panel will control the operation of test system.

13. Test Number - A three-decimal digit display of the number of the test currently being performed.

14. Time Delay in Progress - Single display which is illuminated whenever the test system is instructed to perform a time delay.

15. Parity Error - Illuminates whenever a parity error is detected within the computer/controller.

16. Switching Verification Error - Illuminates whenever a switching verification is not achieved.

17. Arithmetic Overflow - Illuminates whenever an overflow occurs in an arithmetic operation.

18. Measurement in Progress - Single display which is illuminated when the test system is performing a measurement.

c. Maintenance Panel

The maintenance panel contains the controls and displays provided as an aid to the operator in maintaining the test system.

1. Mode Switch - This seven position switch places the computer/controller in the Automatic Test, Magnetic Tape to Memory, Paper Tape to Memory, Memory Test, Data Repository, Paper Tape Test, or Manual Test mode of operation.

2. Mode Display - Displays the mode selected by the Mode Switch

3. Start Pushbutton - Starts the test system operations of the mode selected by the Mode Switch.

4. Computer Submode Switch - This three-position switch places the computer in the Normal, Single Computer Instruction, or Single Clock submode.

5. Computer Submode Display - Displays the sub-mode selected by the Computer Submode Switch.

6. Controller Submode Switch - This three-position switch places the controller in the Normal, Single Controller Character, or Single Controller Pulse submode.

7. Controller Submode Display - Displays the submode selected by the Controller Submode Switch.

8. Memory Mode Switch - This four-position switch places the computer in the Run, Verify, P-Count, or Interrupt Address mode. The Run position is the normal operating position. The Verify position allows the operator to check the contents of the memory after it has been loaded by paper tape. To accomplish this, the operator will run the paper tape through a second time. If the contents of the memory does not compare with the contents of the tape, the verify process stops at the memory address in which the error was detected. The P-Count position allows the computer to advance the program counter to an address specified by the Interrupt Address Switches without performing any instructions. The Interrupt Address position allows the computer to perform the instructions of the program and then to stop the program at an address specified by the Interrupt Address Switches.

9. Memory Mode Display - Displays the mode selected by the Memory Mode Switch.

10. Interrupt Address Switches - Four rotary "digi" type switches select the memory address (0000-7777) at which the computer operation will be stopped. (Control and Display)

11. Unit Under Test Address Switches - Four rotary "digi" type switches (0000-9999) allow the maintenance technician to search the magnetic tape for the test program for any unit under test. (Control and Display)

12. Block Address Switches - Two rotary "digi" type switches (00-99) allow the maintenance technician to search the magnetic tape for any particular block of data within a test program for a unit under test.

13. Instruction Display - Displays the instruction under which the computer and/or controller is currently operating.

d. Manual Input

The manual input consists of a keyboard which allows the operator to manually control the operation of the controller when in the Manual Test mode of operation. From this keyboard the operator can insert any desired controller test sequence a character at a time as well as punch on the paper tape punch any desired set of Fieldata characters.

e. Test Results

In addition to the panel displays required for ordinary computer/controller operation and maintenance, certain visual displays for operator use are necessary. The test result indicators will display the function, magnitude, and range of the last measurement of the test system. Included with this display will be the GO, HIGH, LOW test result indicators. These indicators will be addressed by use of a

Store instruction together with a unique output address. The visual indication will persist until reset when a new measurement is performed.

f. Printer

The printer provides a hard copy of the results of the tests performed, the status of the unit under test, the status of the test system, complete data on a component that has failed, and any manual operations that must be performed by the operator.

A.2.2 CONTROL OF THE COMPUTER/CONTROLLER

The operations of the Computer/Controller are controlled in two ways. The main control is exercised by the use of one of the seven modes of operation. To obtain semiautomatic control of the C/C operations, one of four submodes may be utilized.

A. Modes of Operation

The seven modes of operation are:

(1) Automatic Test
(2) Magnetic Tape to Memory
(3) Paper Tape to Memory
(4) Test from Memory
(5) Data Repository
(6) Paper Tape Test
(7) Manual Test

a. Automatic Test

The Automatic Test mode is the normal operating mode of the Computer/Controller. This mode is used for either automatic or semiautomatic testing of units-under-test. In this mode the required test program is located, placed in memory, and then performed under the direction of the Computer/Controller.

When this mode is selected, the Computer/Controller determines automatically, from coded data input by the unit under test adaptor cable or from the unit under test address switches, the address of the preprogrammed data on magnetic tape which contains the test sequence for the unit-under-test.

The C/C then directs a search of the magnetic tape to locate the block of data which has the desired address. The length of the test program may require that more than one block of data be used to completely test the unit under test. Each of these blocks is assigned a number according to its sequential position in the test program. Every block of data on the magnetic tape has a unique address; this address consists of the number assigned to the unit under test and the number of the block. The blocks are arranged on the magnetic tape with the addresses on the tape increasing in magnitude as the tape is scanned in the forward direction.

The C/C causes the tape to be searched in the forward direction until a block address is read. If the address is less than the desired value, the search continues in the forward direction until the desired block is located. If the first address read is greater than the desired value, the C/C causes the tape to be scanned in the reverse direction until the desired block of data is located; at this time the C/C causes search to be performed in the forward direction until the desired block is again located.

Once the proper block of test data is located, the C/C causes the entire block to be loaded into the memory of the computer. After the loading is completed, the computer performs the operation of the instructions which were just placed in memory.

The C/C performs the test program automatically, including the search for additional blocks of data, until the UUT is judged to be working or until a faulty item has been identified.

B. Magnetic Tape to Memory

The MTTM mode permits the transfer of one block of data from the magnetic tape to the core memory. This mode is utilized mainly as

a maintenance function to eliminate problems which occur in transferring data into the memory.

When this mode of operation is selected, the C/C determines automatically, from coded data, the address of the block which is to be loaded into the memory.

The C/C then directs a search of the magnetic tape, utilizing its bi-directional search capability, until the desired test block is located. The memory is then loaded with the data of the block.

c. Paper Tape to Memory

The PTTM mode permits the memory of the C/C to be loaded with data from a punched paper tape. The paper tape to be loaded must be positioned on the tape reader so that reading in the forward direction will present the data to the tape reader.

This mode is utilized to permit operator-prepared test programs to be placed in the memory. This function is mainly for maintenance.

The C/C does not search for a particular block of data but scans in the forward direction until the beginning of data is recognized. The data following on the punched paper tape is then loaded into the memory.

d. Test from Memory.

The Test from Memory mode permits one block of a test program to be performed on the unit under test. When this mode is selected, the C/C performs the test program which is then stored in the computer memory stopping when additional programs are called for.

This mode is utilized in maintenance and program debugging functions performed by the operator.

e. Data Repository

The Data Repository Mode is utilized to generate a record on magnetic tape of the tests performed that day on the various UUTs. As each test is performed on the UUTs, the C/C punches the test result data on paper tape.

When this mode is selected, the C/C directs the reading into memory of blocks of test result data from the punched paper tape. When an entire block has been read in, the C/C writes the data from memory onto the magnetic tape unit which is used as the data repository. After this writing is completed, the C/C reads in another block of test data from the paper tape and repeats the above read-write cycle until the entire test results of the day have been placed on magnetic tape.

f. Paper Tape Test

The Paper Tape Test mode is utilized when performing maintenance functions. The use of this mode allows test routines to be read directly from paper tape to the controller portion of the C/C (bypassing the computer operations).

When this mode is selected, the paper tape reader scans the paper tape program in the forward direction until the beginning of data is recognized. The test program is then performed sequentially.

g. Manual Test

The Manual Test mode is utilized to manually control the controller functions of the C/C by using a Manual Input keyboard. The prime use of this mode is to perform maintenance functions; an additional use is to perform emergency tests on UUTs if the computer functions of the C/C are not operating

When this mode is selected, the operator is able to generate test programs for the controller by depressing the proper character keys on the Manual Input keyboard. As each key is depressed, the controller receives the Fieldata code representing that character. The controller interprets each character as either a command or as data. The controller performs the functions of the command character which is being acted upon in the same manner as if the character were coming from the computer. Each character received by the controller in this mode is printed by the Printer to feed back to the operator the character selected.

In using this mode the operator is able to manually set up and apply any stimulus, select and scale any measurement device, select any test point for monitoring by the Measurement Group, and cause a measurement to be performed.

The operator can also manually control the other assemblies of the controller when in this mode, but would not normally do so.

B. Sub-Modes of Operation

The four sub-modes of operation of the Computer/Controller are:

(1) Single Computer Instruction
(2) Single Clock
(3) Single Controller Character
(4) Single Controller Pulse

The C/C is capable of either entering a sub-mode, exiting from a sub-mode, or exiting to another sub-mode at any point in the test program.

a. Single Computer Instruction

The single computer instruction sub-mode permits the operator to proceed through the test sequence store in memory on an instruction to instruction basis. This sub-mode is operational only when the computer is directing the functions of the test program as in the Automatic Test or Test From Memory modes.

When this sub-mode is selected, the computer performs normally except that after each instruction is read from memory and decoded, the operations are interrupted. The operator then causes the computer to perform the functions of that instruction and extract the next instruction from memory by depressing the Proceed pushbutton. This single instruction sequencing may continue for the entire test program or any portion of it except during read or write operations with magnetic tape.

b. Single Clock

The single clock pulse sub-mode permits the operator to proceed through the computer operations on each instruction on a clock pulse by clock pulse basis.

When this sub-mode is selected, the operations of the computer are interrupted after each pulse of the computer clock. To continue to the next computer operation, the operator must depress the Proceed pushbutton; this action allows one clock pulse to be generated.

c. Single Controller Character

The single controller character sub-mode permits the operator to control the flow of information and commands into the controller portion of the C/C. This sub-mode is operational in any of the modes when data is being read into the controller, such as the Automatic Test, Test from Memory, or Paper Tape Test modes.

When this sub-mode is selected, the operations of the controller are interrupted after each character is received by the controller. The operations required upon the character and the receipt of a new character are initiated by an operator depression of the Proceed pushbutton.

d. Single Controller Pulse

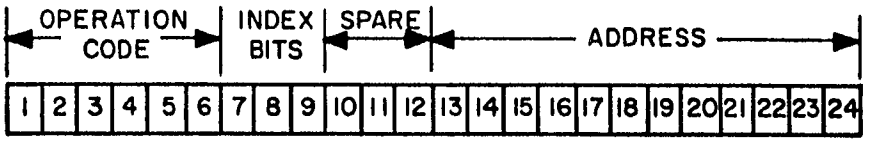
The single controller timing pulse sub-mode permits the operator to control the operations performed upon the controller characters on a timing pulse by pulse basis. This sub-mode is operational in any of the modes when data is being read into the controller such as the Automatic Test, Test from Memory, or Paper Tape Test modes.

A.3 COMPUTER/CONTROLLER LANGUAGE

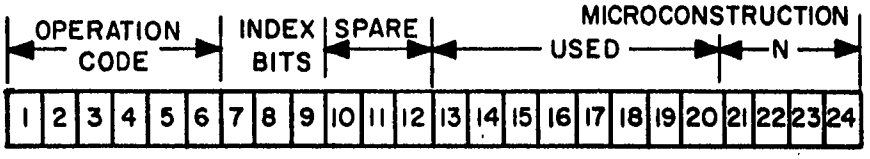
The instructions for the computer/controller are divided into two groups: those that direct the sequence of operations in the computer, as interpreted by the Control Unit, and those that direct the sequence of operation in the Controller, as interpreted by the Control Director. The computer controls the flow of data to and from the High-Speed Memory. When the test procedures require controller functions to be performed, a Write instruction is programmed. This computer instruction transfers data to the controller over a single character data bus. The data transferred consists of the controller instruction characters and their required data characters

A.3.1 COMPUTER INSTRUCTION REPERTOIRE

The computer uses a 24-bit instruction word whose format is variable depending on the function to be performed. The most common formats are shown in Figure A-2 A brief description of the functions of these formats is given below



FORMAT A



FORMAT B

Figure A-2. Instruction word format

A. Operation Code

The operation code is a numerical representation of an instruction in the octal number system. An alphabetic code is utilized by the programmer to identify an instruction and is called a mnemonic code. The mnemonic code is readily translated by the programmer to the optimized operation code of the computer. Two three-digit octal numbers make up the operation code.

B. Index Bits

The index bits in an instruction word are used to select one of three index registers whose contents modify the address portion of the instruction. When an index bit appears in instructions that can be modified, the contents of the selected index register are added to the address portion of the instruction. The instruction is then executed as if its address portion had contained the stated address plus the contents of the index register. The index modification adds 12 microseconds to the execution time of the instruction.

The index registers may also be used as counters when addressed by a "Jump Index" instruction. This operation is described under the definition of the "Jump Index" instructions.

C. Spare Bits

The three spare bits provide a means for expanding the memory size in modular blocks.

D. Address

The address portion of an instruction specifies the location in a storage unit to which access will be made during the execution of the instruction. The storage unit may be internal (High-Speed Memory) or external.

The computer uses the twelve least significant bits of the instruction word as the address bits. These bits are divided into four octal numbers with up to 4096 possible combinations in the range of 0000 to 7777.

Table A-1. List of computer instructions

Instruction	Instruction Execution Time (Microseconds)
Clear and add	24
Add	24
Subtract	24
Multiply	84
Divide	84
Store	24
Extract	24
Set Index	24
Jump Exit	36
Jump Return	24
Jump on Negative	12
Jump Unconditional	12
Jump Index	24
Jump on Overflow	12
Clear Accumulator	12
Clear Q-Register	12
Clear Program Counter	12
Logical Left Shift	12-36
Logical Right Shift	12-36
Algebraic Right Shift	12-36
Algebraic Left Shift	12-36
Exchange Registers (A and Q)	12
Logical Sum (A and Q)	24
Add A and Q and Leave in A	24
Add A and Q and Leave in Q	24

Table A-1 (Continued)

Instruction	Instruction Execution Time (Microseconds)
Round	12
Add one to A	12
Ones Complement of A	12
Twos Complement of A	12
Make A Negative	12
Make A Positive	12
Read	Indeterminate
Write	Indeterminate
Program Halt	12

E. Microinstruction

The twelve bits in format B, denoted "microinstruction", indicate those bits used for a subsidiary operation code when the normal operation code (bits 1-6) contains all zeros. These microinstructions do not require an explicit address and are performed as subdivisions of the single all zeros instruction, command control.

F. Instruction Definition

The instruction repertoire of the Computer contains many features usually found only in large scale data-processing equipment. Table A-1 contains the English language name for the instruction and the instruction execution time. The following paragraphs give a brief description of each of the instructions, taken in the order shown in the table.

a. Clear and Add

The content of the specified memory location is placed in the accumulator. The original content of the accumulator is placed in the Q-register. The content of the Q-register is lost. The content of the memory location is not changed. (Format A)

b. Add

The content of the memory location specified by the address part of the instruction is added to the content of the accumulator. The sum is left in the accumulator. The contents of the Q register and data memory are not changed. For the correct sum, the following condition must be met: $-1.0 \leq \text{sum} < +1.0$. If the condition is not met, an overflow is registered. (Format A).

c. Subtract

The content of the memory location specified by the address part of the instruction is subtracted from the content of the accumulator. The difference is left in the accumulator; the contents of the Q-register and data memory are not changed. For the correct difference the following condition must be met: $-1.0 \leq \text{difference} < +1.0$. If the condition is not met, an overflow is registered. (Format A)

d. Multiply

The content of the memory location specified by the address part of the instruction is multiplied by the content of the accumulator. The product is left in the accumulator and Q-register as a signa and 46 numeric bits. The least significant bit of the Q-register contains the sign bit of the multiplier. The content of the memory is not changed. The original contents of the accumulator and Q-register are destroyed. (Format A).

e. Divide

The content of the memory location specified by the address part of the instruction is divided into the combined contents of the accumulator and Q-register. The quotient is left in the accumulator as sign plus 23 numeric bits. The least significant bit of the quotient is set to one (not added). The final remainder is not formed. The dividend is destroyed, the content of the memory is not changed. (Format A)

f. Store

The content of the accumulator is transferred to the memory. location specified by the address part of the instruction. The original content of the specified memory location is destroyed. The contents of the accumulator and Q-register are not changed. (Format A).

g. Extract

The content of the location specified by the address part of the instruction is used as a mask to delete bits from the content of the accumulator. For every bit position in the mask which is a zero, the corresponding list in the accumulator is reset to zero. The result is left in the accumulator. The contents of the Q-register and memory are not changed. (Format A)

h. Set Index

The address part of the instruction is transferred to the index register specified by the tag bits of the instruction word. The original content of the index register is destroyed. The accumulator, Q-register and memory are not changed. (Format A)

i. Jump Exit

Jump Exit is a two address jump instruction using two consecutive memory locations. The first of these locations contains the Jump Exit

instruction code and an address specifying a memory location where the program return-address is to be stored. The program return-address is the address of the location following the two word Jump Exit instruction. The second location specifies the memory location to which a jump is executed. (Format A)

j. Jump Return

The program executes a jump to the memory location whose address iscontained in the memory location specified by the address part of the instruction. This instruction is thus an indirect address type instruction. The contents of memory, the accumulator and Q- register are not changed. The Jump Exit, Jump Return faculty enables the addressing of a specific subroutine from different locations throughout a progrm and the returning to the next sequential location to that from which the jump was originally made. (Format A)

k. Jump on Negative

If the sign position of the accumulator contains a one, signifying a negative number, the program executes a jump to the memory location specified by the address part of the instruction. If the accumulator is positive, i.e., if the sign position contains a zero, the program steps to the next memory location. The contents of the accumulator and Q-register are not affected. (Format A)

l. Jump Unconditional

This instruction causes the computer to take its next instruction from the location specified by the address part of the instruction. The contents of the accumulator and Q-register are unchanged. (Format A)

m. Jump Index

If the content of the selected index register is not zero, the program executes a jump to the memory location specified by the address part of the instruction. If the content of the selected index register is zero, the program steps to the next memory location. In either case, one is algebraically subtracted from the content of the selected index register after the test. The contents of the accumulator and the Q-register are not changed. The tag bits specify the index register to be used. (Format A)

n. Jump on Overflow

The Jump on Overflow instruction causes a jump to the address specified by the address part of the instruction if the overflow bits is set. After the test has been made, the overflow bit is reset. Overflows occur during the Add and Subtract instructions only, when the result exceeds the machine numbering system. (Format A)

o. Clear Accumulator

The accumulator is reset to zero. The content of the Q-register is not changed. (Format B)

p. Clear Q-Register

The content of the Q-register is reset to zero. The content of the accumulator is not changed. (Format B)

q. Clear Program Counter

The program counter is reset to zero. The contents of the accumulator and the Q-register are not changed. Effectively, program control executes an unconditional jump to memory location 0000. (Format B)

r. Logical Left Shift

In the Logical Left Shift instruction, the accumulator and Q-register are joined together and shifted left up to 12 times, the number of shifts depending on the state of the 4 least significant bits of the address portion of the instruction. (The four address bits contain a weighted code such that the most significant bit means 5 shifts; the next bit, 4 shifts; the next bit, 2 shifts; and the least significant bit, 1 shift.) Bits leaving the sign bit position of the accumulator are entered into the least significant bit position of the Q-register. (Format B)

s. Logical Right Shift

The Logical Right Shift instruction shifts the combined A and Q-registers right n times, where n is determined by the four least significant bits of the address part of the instruction (See Logical Left Shift). Zeros are shifted into the sign position of the accumulator. Bits leaving the least significant bit position of Q are lost. (Format B)

t. Algebraic Right Shift

Algebraic Right Shift instruction shifts the combined A and Q registers right n times, the number of times depending on the four least significant bits of the address portion of the instruction. (See Logical Left Shift) Whatever is in the sign bit position of the accumulator will be shifted right n times and also left in the sign position. Bits leaving the least significant bit position of Q- are lost. (Format B)

u. Algebraic Left Shift

Algebraic Left Shift shifts the combined A and Q registers left n times, the number of times depending on the state of the four least significant bits of the address part of the instruction (see Logical Left Shift). The sign bit of the accumulator is not disturbed. Bits leaving the next most significant bit position are lost. Zeros enter the least significant bit position of Q. (Format B)

v. Exchange A and Q

The content of the accumulator is transferred to the Q register. The content of the Q register is transferred to the accumulator. (Format B)

w. Logical Sum of A and Q

The content of the accumulator is logically added to the content of the Q register. For every bit in the accumulator that contains a one (1), the corresponding bit in the Q register is complemented (the complement of zero is one and conversely, the complement of one is zero). All other bits in the Q register remain unchanged. The logical sum is placed in the accumulator. The original content of the accumulator is placed in the Q register. The original content of the Q register is lost. (Format B)

x . Add A and Q and Leave in A

The content of the accumulator is added to the content of the Q register;; the sum is left in the accumulator. The original content of the accumulator is placed in the Q register. The original content of the Q register is lost. (Format B)

y. Add A and Q and Leave in Q

The content of the accumulator is added to the content of the Q register. The sum is placed in the Q register. If a carry from the most significant stage is present, the carry bit is left in the least significant bit position of the accumulator. The remainer of the accumulator is rest to zero. (Format B)

z. Round

If the most significant bit position of the Q register contains a 1, a logical one in the least significant bit (2^{-23}) is added to the accumulator and

carries are propagated through the accumulator if generated. The content of the Q register is not changed. (Format B)

aa. Add One to A

The content of the accumulator is increased by the addition of 2^{-23}. The content of the Q register is not changed.(Format B)

bb. One's Complement of A

The one's complement of the content of the accumulator is formed and left in the accumulator. The content of the Q register is not changed. (Format B)

cc. Two's Complement of A

The two's complement of the content of the accumulator is formed and is left in the accumulator. The content of the Q register is not changed. (Format B)

dd. Make "A" Negative

The content of the accumulator is made negative in two's complement form. If the original content is already negative, there is no change. The content of the Q register is left unchanged. (Format B)

ee. Make "A" Positive

The content of the accumulator is made positive. If the original content is already positive, there is no change. The content of the Q register is left unchanged. (Format B)

ff. Read

The "Read" instruction is a two address instruction using two consecutive memory locations. The first of these locations contains the "Read"

instruction code and an address of a peripheral device. The second word specifies the number of words to be transferred and the memory address for the first of the sequenced words.

In a "Read" instruction, characters are read and assembled into words by the input/output buffer.

gg. Write

The "Write" instruction is a two address instruction using two consecutive memory locations. The first of these locations contains the "Write" instruction code and an addres of a peripheral device. The second word specifies the number of words to be transferred from sequential memory locations and the memory address from which the first word is to be read.

In a "Write" instruction, words are read from memory and separated into four six-bit characters per word and then transferred out serial-by-character by the input/output buffer.

hh. Program Halt

The "Halt" instruction stops the reading and execution of computer instructions. When the program halt occurs, the operation register contains the "Program Halt" instruction code and the accumulator and other computer registers remain at their last readings. When the proceed button is pushed, the execution of instructions continues from the next memory location unless the program counter has been advanced under console control to a different location.

A. 3. 2 CONTROLLER INSTRUCTIONS

The controller uses a single character instruction word in its operations. The six least significant bits of a Fieldata character are used for the operation code. The controller instruction word consists wholly of the operation code, with the address of the instruction being implied.

The control director is capable of interpreting 20 mnemonic instructions; however, five of these instructions are utilized only with simple controller systems and not the computer/controller system described herein. Table A-2 contains the mnemonic operation code, the English language name for the instruction, and the six bits of Fieldata code. The following paragraphs give a brief description of each of the instructions, taken in the order shown on the chart.

A. Switching Follows (S)

This instruction signifies that the characters following it compose mnemonic switching words which are to be routed to the switching control buffer. The switching words contain the stimulus, measurement, and test point set-up instructions. Each of the switching words consists of at least 4 characters, but not more than 12 characters. The number of switching words, following thin instruction is not limited. The first character of each switching word is restricted to one of the alphabetical characters. The fifth through twelfth characters of each switching word are restricted to those Fieldata characters which have zone bits of 10 and 11. These restrictions enable the controler to determine the beginning of each switching word. An entire switching word is stored in the Switching Control Buffer before being used to set up the desired function. After performing the desired operations on the switching word, a new word is stored in the Switching Control Buffer. The operation of storing switching words and performing their operations continues until an Item Separator command is recognized.

Table A-2. Controller Instructions

Mnemonic Code	Instruction	FIELDATA Characters
S	Switching Follows	011000
P	Print	010101
Z	Print and Punch	011111
M	Measure	010010
C	Continuous Measurement	001000
N	Load Test Number	010010
D	Delay Magnitude	001001
T	Timer Start	011001
E	End Delay	001010
X	External Start	011101
R	Switching Reset	010111
A	Apply	000110
H	Halt	001101
I	Program Interrupt	001110
•	Item Separator	111110
*	Address Follows	101000
V(1)	Print Measurement	011011
U(1)	Compare Upper	011010
L(1)	Compare Lower	010001
F(1)	IF	001011
K(1)	Sub-Address	010000

(1) These instructions are not utilized in the computer/controller system.

B. Print (P)

This instruction routes the characters following it to the Printer via the Printer Control Unit. The operations of this instruction are terminated by the recognition of the Item Separator instruction.

The Printer has twenty print columns which must be discretely selected to control the position in which each character is printed. The control director causes the characters to be printed in the proper column. The printer control causes the paper to be advanced in the printer under command from the test program or after printing in the twentieth column.

C. Print and Punch (Z)

This instruction routes the characters following it to both the Printer Control Unit and the Punch Control Unit. The operations of this instruction are terminated by the recognition of the Item Separator instruction by the control director. Each character is printed in the proper columns by the Printer Unit. The Punch Control Unit generates the proper control and parity bits required to generate a Fieldata character for each character, and causes the complete character to be punched.

D. Measure (M)

This instruction signifies that the Measurement Subsystem is to evaluate the parameter at its input and then present the results in binary-coded decimal form as its output. The Computer/Controller system operation is interrupted until the measurement subsystem signifies that the evaluation is complete. Upon receiving this instruction, the control director generates an evaluate pulse which is routed to the Measurement Group. After completing its evaluation of the parameter at its input, the Measurement Group generates an end evaluation pulse.

E. Continuous Measurement (C)

This instruction signifies that the Measurement Group is to perform repeated evaluations of the parameter at its input. The Computer/Controller operations are interrupted and a positive action is required by the operator before the Computer/Controller operations continue.

After each evaluation has been completed, the control directer provides a one-half second delay and then generates another evaluate pulse, which is routed to the Measurement Group. This operation continues until the operator depresses a Proceed pushbutton.

F. Test Number (N)

This instruction states that the first three characters following it are to be stored in the test number display register. This gives the controller the capability to identify tests within the test program stores in the computer memory.

G. Delay Magnitude (D)

This instruction signifies that the first five characters following it compose the time base and magnitude of the desired time delay. The magnitude of the time delay is programmed most significant digit first and has a range of 0000 to 9999. The first character received over the single character data bus following the instruction character represents the desired time base. The Time Delay Unit utilizes this character to select one of four discrete time bases.

Character Value	Time Base
1	1 microsecond
2	1 millisecond
3	1 second
4	external

The next four characters received over the single character data bus will be the magnitude of the desired time delay.

H. Timer Start (T)

This instruction initiates the time delay whose magnitude has been previously selected by the "Delay Magntude" instruction. The controller operation is not interrupted by the initiation of the time delay. This instruction is always utilized in conjunction with the "End Delay" instruction.

The Time Delay Unit upon receipt of a time delay start pulse, starts the time delay. When the time delay is over, the Time Delay Unit generates an end time delay signal.

I. End Delay (E)

This instruction always follows the "Timer Start" instruction; either directly or after other functions have been performed. It examines the output of the Time Delay; if the time delay is over, the controller operation is interrupted until the time delay is complete.

J. External Start (X)

This instruction aliows the controller to accept an external time delay start pulse; when the time delay (magnitude selected by the "Delay Magnitude" instruction) is over, the controller performs an immediate evaluation of a parameter by the Measurement Group. The Computer/ Controller operation is interrupted until the operations of this command are complete.

K. Switching Reset (R)

This instruction is utilized to reset all the functions which are set up by the Switching Control Buffer.

A switching reset pulse is routed to the Measurement and Stimulus Subsystem for resetting all functions to their normal OFF condition.

L. Apply (A)

This instruction is utilized to simultaneously connect all of the stimuli, which have been previously set up, to the unit under test through the monitor/adapter cables. The apply pulse is routed to the Stimulus Group for simultaneous closing of the application relays of all the stimuli which have been previously set up.

M. Halt (H)

This instruction is utilized to end the testing of a unit under test. Upon recognizing this instruction, the control director generates a switching reset pulse and a reset pulse. The reset pulse places the Computer/Controller in a standby condition and resets all of the digital circuitry.

N. Program Interrupt (I)

This instruction is utilized to interrupt the subsystem operation to allow the operator to perform any required manual test functions. Operator instructions will have been previously given to the operator via the Printer.

A positive action is required before the Computer/Controller operation will continue. The operator is required to depress a Proceed pushbutton, which removes the control exercised by this instruction.

O. Item Separator (•)

This unique character, when recognized by the control director, terminates the operations of any instruction being performed under the direction of the control director. This is a unique command, in that the Fieldata character chosen to represent this command is not utilized for any other function or as a data character.

P. Address Follows (*)

This instruction is utilized to identify the address of each block of data on magnetic tape. This instruction is interpreted by the input/output buffer when data is being searched on magnetic tape. It utilizes a unique Fieldata character that does not represent any other data character.

The five instructions which are not described (Print Measurement, Compare Upper, Compare Lower, IF, and Subaddress) are utilized in simple controller systems which contain a Tape Search Unit and Digital Comparator. These instructions are not removed from the control directors capability due to building block philosophy, which states that when reconfiguring different systems, design changes should be kept to a minimum.

A. 4 MEASUREMENT SELECTION AND STIMULI CONTROL

The interface between the control equipment and the stimulus, test point selection, and measurement equipment is accomplished by means of a Switching Control Buffer. The function of the Switching Control Buffer receives switching instructions from either manual or automatic control equipment, selects the proper unit of stimulus or measurement equipment to be operated upon, and sets up the proper magnitude and type of function within that equipment.

A. 4. 1 PROGRAMMING LANGUAGE

Programming switching instructions for the selection of the proper stimuli and measurement is one of the major portions of the overall programming task, since at least one of these functions must be set up or changed for every test performed. In the past, such programming has been accomplished by utilizing detailed code books with flow charts, code sheets and detailed programming instructions. In many cases, compiler or conversion routines were necessary to machine-orient the

instructions. A need has long existed for a less cumbersome and time-consuming method of accomplishing the stimulus and measurement selection control. For this reason RCA has developed a simplified programming language that allows the program to be written in actual alphabetic abbreviations and decimal magnitudes of the desired functions to be selected. For example, to select a magnitude of + 375 volts from a dc power supply, the instruction +375 might be programmed. This programming language is known as "Simplified Language for Automatic Test Equipment" or SLATE.

In utilizing SLATE to program a given test sequence, the only information needed is a list of the available stimuli and measurement functions with their characteristics and abbreviations. SLATE also lends itself to direct modification by arithmetic processes; i.e., the instruction +375 might be modified by adding the decimal number 7 to it, thus producing the instruction +382. The resulting instruction would select +382 volts from the same dc power supply.

A typical SLATE switching instruction or "switching word" contains all the information necessary to select uniquely a particular stimulus or measurement function and to set up the magnitude of that function. The switching word is composed of three main parts: an address, a subaddress, and a magnitude. The exact format of the switching word can easily be tailored to suit the requirements of a particular equipment design.

In determining the exact format to be used, a number of factors must be taken into consideration: the functions to be controlled, standardization of equipment, cost, flexibility, and simplicity.

The three basic functions to be controlled by the switching word are:

(1) Selection and application of type and magnitude of stimulus

(2) Selection of proper test points

(3) Selection of type and range of measurement.

Standardization can be achieved by choosing a method of switching control which would allow identical chassis to be freely interchangeable and yet uniquely selected.

The cost of implementing a given format is a function of the cost of programming, design effort, and the switching control hardware necessary to mechanize that format. These costs apply not only to the Switching Control Buffer, but also to each of the controlled chassis and the program control equipment. The selection of the exact switching word format should be made in such a manner that the overall costs be kept to a minimum and yet satisfy all the other requirements.

The format must be flexible enough to satisfy the control requirements of a wide variety of controlled functions. Consideration should also be given to possible future test applications without significant changes or modifications of either the switching word format or the switching control hardware.

The simplicity of the format has a direct affect upon the case of programming and the ease with which the format may be mechanized.

Keeping in mind the above considerations, the details of the switching word format may be developed. In determining the address portion of the format, consideration must be given to the number of functions to be uniquely selected and the ease with which these functions may be

programmed. For example, assume that the number of items to be addressed is approximately 100. If alphabetic characters were used in the address, any one character position in the format could uniquely address 26 functions and two character positions could uniquely address $(26)^2$ or 676 functions. Although 676 possible addresses far exceeds the 100 required, many awkward combinations such as JQ and FZ are not suitable as abbreviations for functions. If an additional alphabetic character position were utilized, $(26)^3$ or 17,576 possible combinations of alphabetic characters would be available from which 100 easily remembered abbreviations of functions may be chosen for unique addresses. The large number of possible combinations would readily provide addresses for any additional functions to be included in future applications.

The sub-address adds to the flexibility of the switching word. For example, the sub-address could be used to control the application relay in a selected stimulus or it could be used to uniquely select one of several available functions or sub-functions within a selected chassis. The sub-address might also be used as an additional magnitude character in certain instances. Flexibility is enhanced by allocating at least one character position as such a sub-address and allowing this position to be programmed by alphabetic, numeric, and perhaps even symbolic characters interchangeably.

The magnitude portion of the switching word format would contain the proper number of decimal character positions to satisfy the requirements of all of the controlled functions. Different types of functions may require a different number of magnitude character positions. For instance, a measurement function might require only one magnitude character, such as in the following instruction: "Measure a dc voltage on the 10^2 range" or MDC 2. A test point selection function might require a few more characters such as in the instruction, "Connect the measurement bus A to test point 193", or TPA 193. A particular

stimulus function may require many characters such as in the instruction, "Set up a CW carrier, the frequency of which is 197.361572 Mc/s," or CWF 197361572.

Since the number of characters required in the switching work varies according to the function selected, either a fixed number of characters must be standardized upon or a method must be devised to determine the end of one group of switching characters and the start of another. The second method is preferred, since it results in a shorter test program and less testing time. Since the first character is always alphabetic and the magnitude characters are numeric, the start of a new switching word can be readily detected.

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